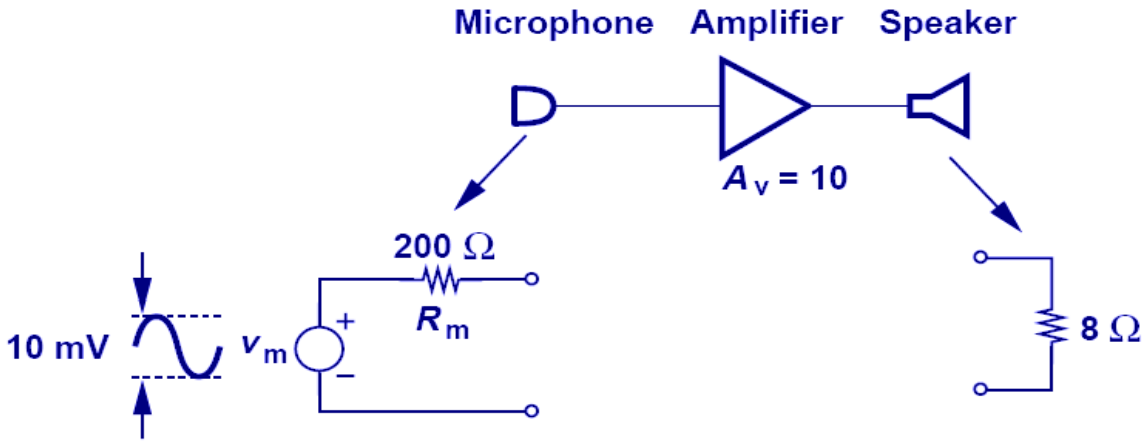
Chapter 5 Bipolar Amplifiers

- 5.1 General Considerations
- 5.2 Operating Point Analysis and Design
- 5.3 Bipolar Amplifier Topologies
- 5.4 Summary and Additional Examples

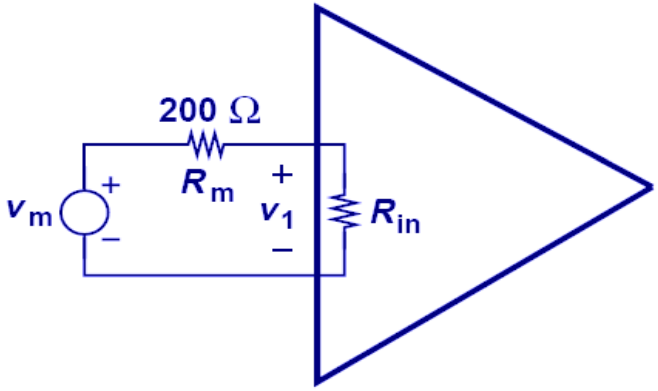
General Concepts	Operating Point Analysis	Amplifier Topologies
• Input and Output Impedances	• Simple Biasing	• Common−Emitter Stage
• Biasing	• Emitter Degeneration	• Common−Base Stage
• DC and Small−Signal Analysis	• Self−Biasing	• Emtter Follower
	• Biasing of PNP Devices	

Voltage Amplifier

- In an ideal voltage amplifier, the input impedance is infinite and the output impedance zero.
- But in reality, input or output impedances depart from their ideal values.



(a)



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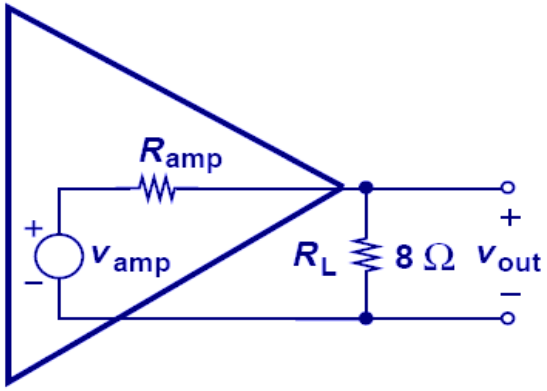


(c)

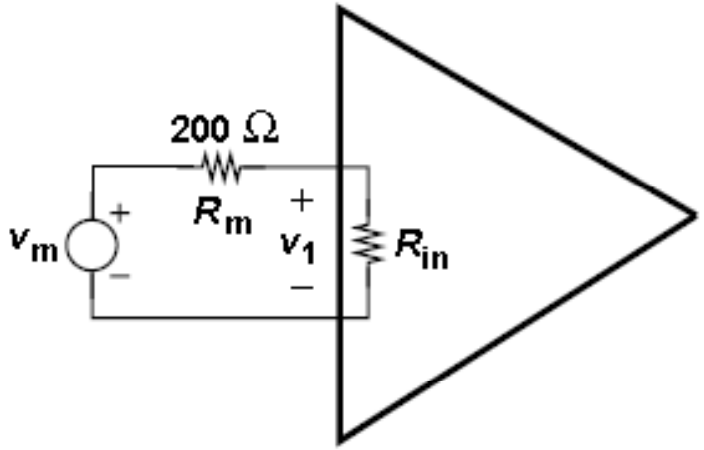
Example 5.1

An amplifier with a voltage gain of 10 senses a signal generated by a microphone and applies the amplified output to a speaker [Fig. 5.1(a)]. Assume the microphone can be modeled with a voltage source having a 10-mV peak-to-peak signal and a series resistance of 200 Ω. Also assume the speaker can be represented by an 8-Ω resistor.
(a) Determine the signal level sensed by the amplifier if the circuit has an input impedance of 2 k Ω or 500 Ω.
(b) Determine the signal level delivered to the speaker if the circuit has an output impedance of 10 Ω or 2 Ω.

Solution

(a) Figure 5.1(b) shows the interface between the microphone and the amplifier. The voltage sensed by the amplifier is therefore given by

$$v_1 = \frac{R_{in}}{R_{in} + R_m} v_m .$$



For $R_{in} = 2$ k Ω,

$$v_1 = 0.91\ v_m$$

only 9% less than the microphone signal level.

Example 5.1 (cnt'd)

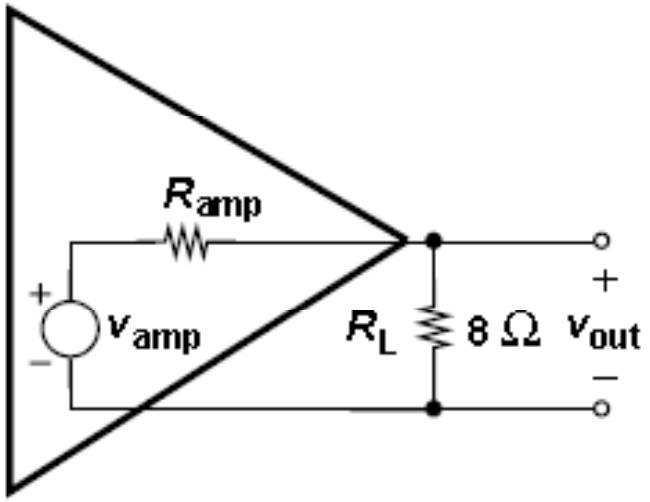
On the other hand, for $R_{in} = 500\ \Omega$,

$$v_1 = 0.71\ v_m$$

i.e., nearly 30% loss. It is therefore desirable to maximize the input impedance in this case.

(b) Drawing the interface between the amplifier and the speaker as in Fig. 5.1(c), we have

$$v_{out} = \frac{R_L}{R_L + R_{amp}} v_{amp}.$$



For $R_{amp} = 10\ \Omega$,

$$v_{out} = 0.44\ v_{amp}$$

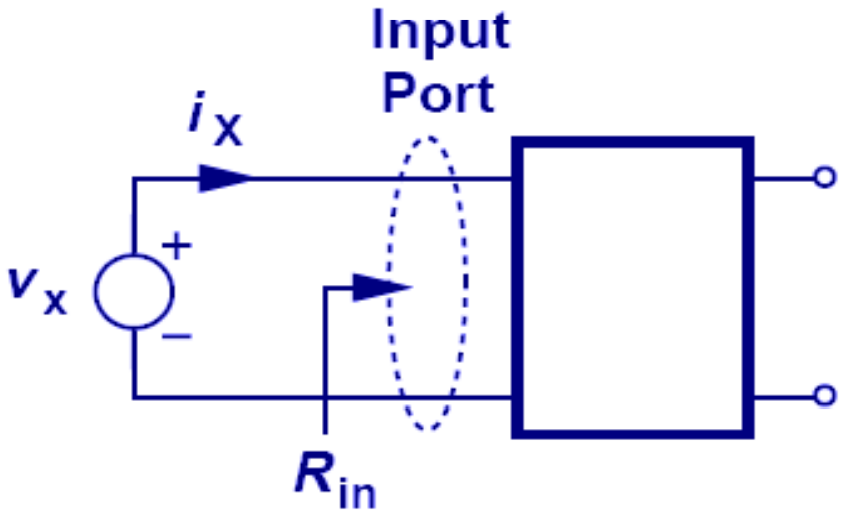
a substantial attenuation. For $R_{amp} = 2\ \Omega$,

$$v_{out} = 0.8\ v_{amp}$$

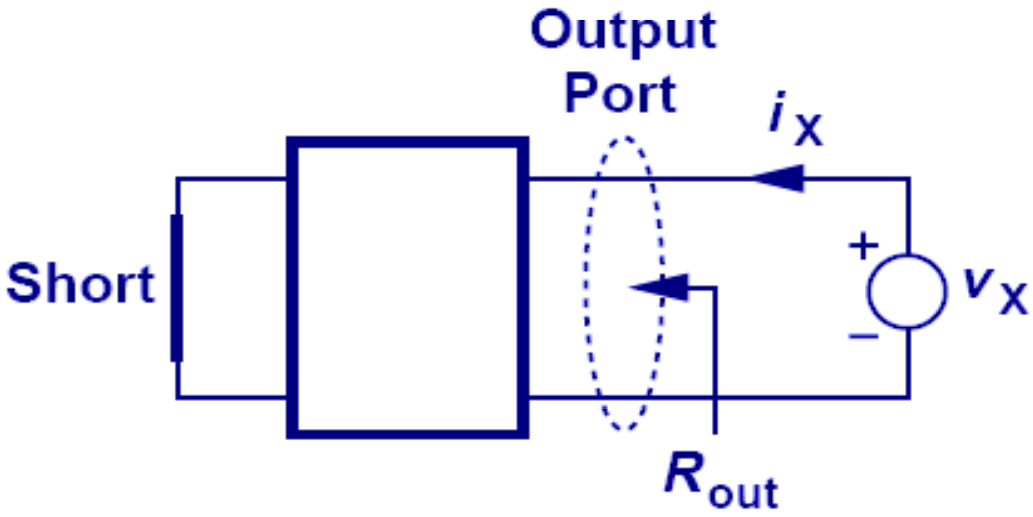
Thus, the output impedance of the amplifier must be minimized.

Input/Output Impedances

- The figures below show the techniques of measuring input and output impedances.
- When calculating input/output impedance, small-signal analysis is assumed.



(a)



(b)

$$R_x = \frac{V_x}{i_x}$$

voltage source is replaced by a short, and current source by an open

Example 5.2

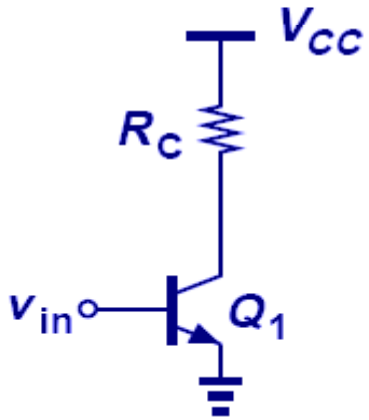
Assuming that the transistor operates in the forward active region, determine the input impedance of the circuit shown in Fig. 5.3(a). .

Solution

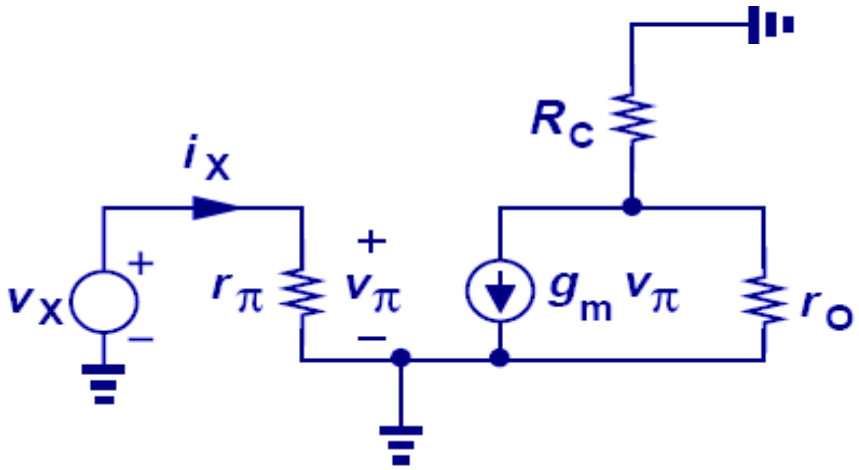
Constructing the small-signal equivalent circuit depicted in Fig. 5.3(b), we note that the input impedance is simply given by

$$\frac{v_x}{i_x} = r_\pi .$$

Since $r_\pi = \beta/g_m = \beta V_T/I_C$, we conclude that a higher β or lower I_C yield a higher input impedance.



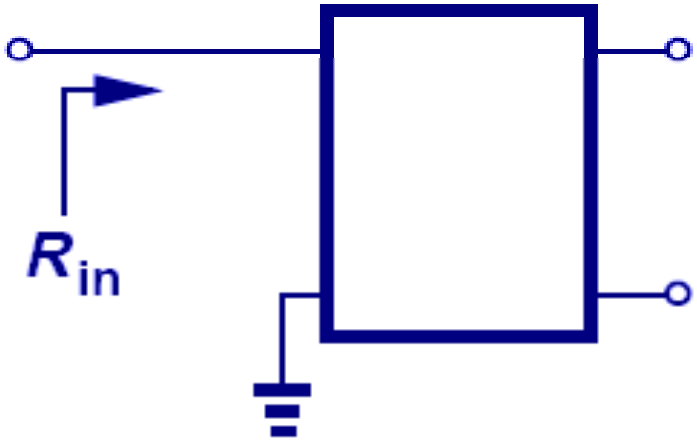
(a)



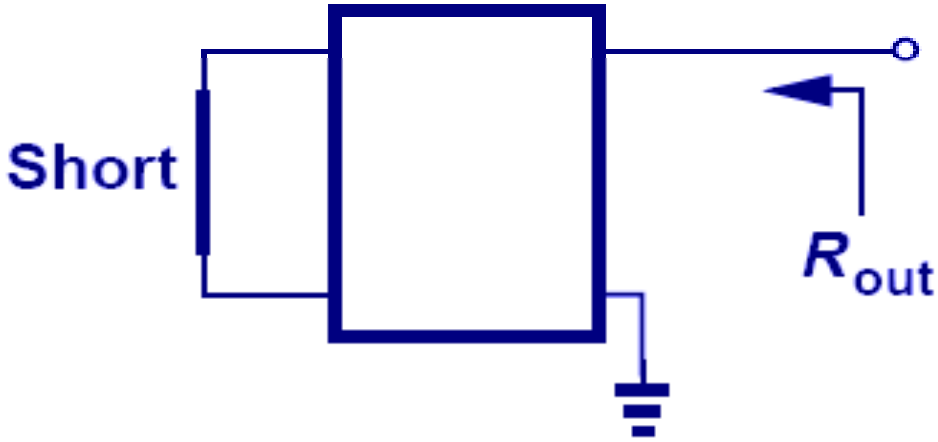
(b)

Impedance at a Node

- When calculating I/O impedances at a port, we usually ground one terminal while applying the test source to the other terminal of interest.



(a)



(b)

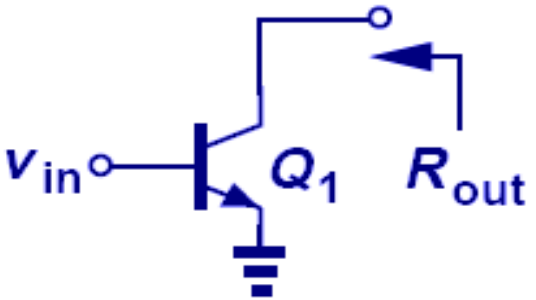
Example 5.3: Impedance at Collector

Calculate the impedance seen looking into the collector of Q_1 in Fig. 5.5(a).

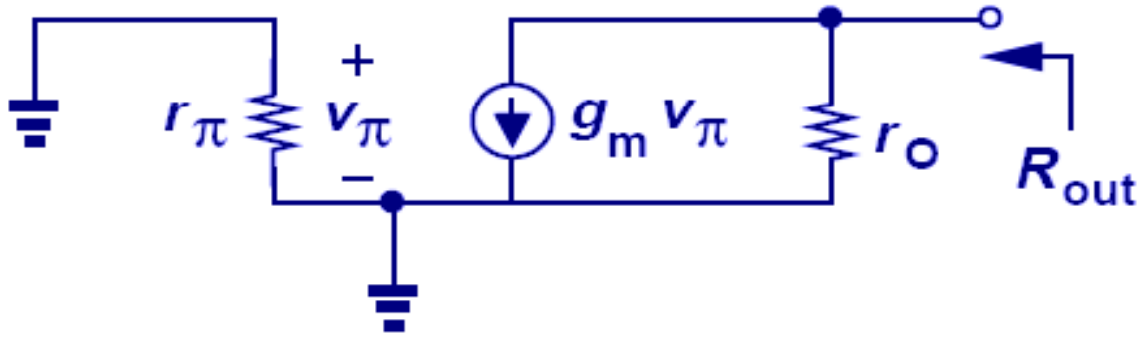
Solution

Setting the input voltage to zero and using the small-signal model in Fig. 5.5(b), we note that $v_\pi = 0$, $g_m v_\pi = 0$, and hence $R_{out} = r_O$.

- With Early effect, the impedance seen at the collector is equal to the intrinsic output impedance of the transistor (if emitter is grounded).



(a)



(b)

Example 5.4: Impedance at Emitter

Calculate the impedance seen at the emitter of Q_1 in Fig. 5.6(a). Neglect the Early effect for simplicity..

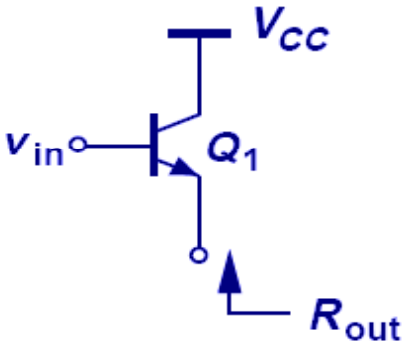
Solution

Setting the input voltage to zero and replacing V_{CC} with ac ground, we arrive at the small-signal circuit shown in Fig. 5.6(b). Interestingly $v_\pi = -v_X$, and

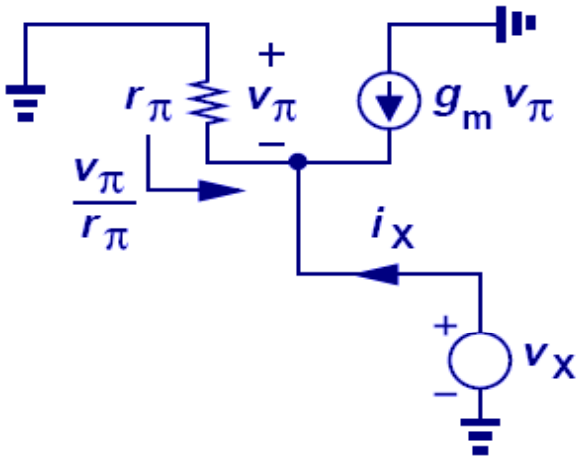
$$g_m v_\pi + \frac{v_\pi}{r_\pi} = -i_X .$$

That is,

$$\frac{v_X}{i_X} = \frac{1}{g_m + \frac{1}{r_\pi}} .$$



(a)



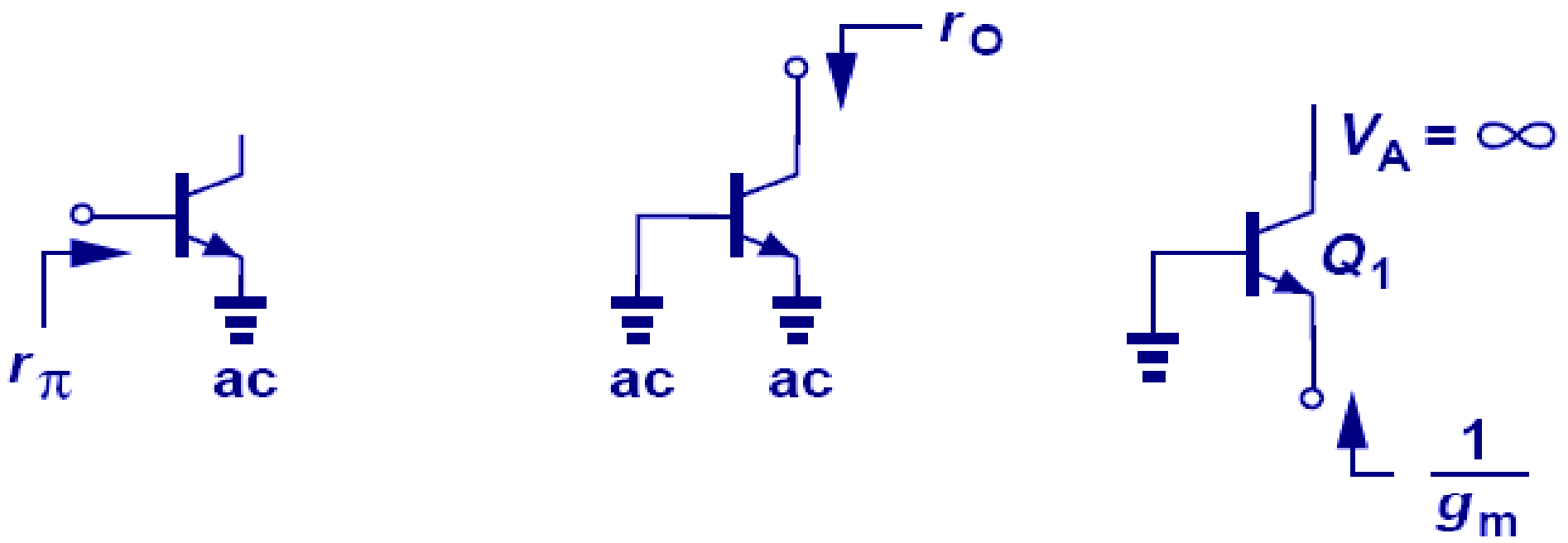
(b)

Since $r_\pi = \beta/g_m >> 1/g_m$, we have $R_{out} \approx 1/g_m$.

- The impedance seen at the emitter of a transistor is approximately equal to one over its transconductance, $1/g_m$ (if the base is grounded).

Three Master Rules of BJT Impedances

- Rule # 1: looking into the base, the impedance is r_π if emitter is (ac) grounded.
- Rule # 2: looking into the collector, the impedance is r_o if emitter is (ac) grounded.
- Rule # 3: looking into the emitter, the impedance is $1/g_m$ if base is (ac) grounded and Early effect is neglected.

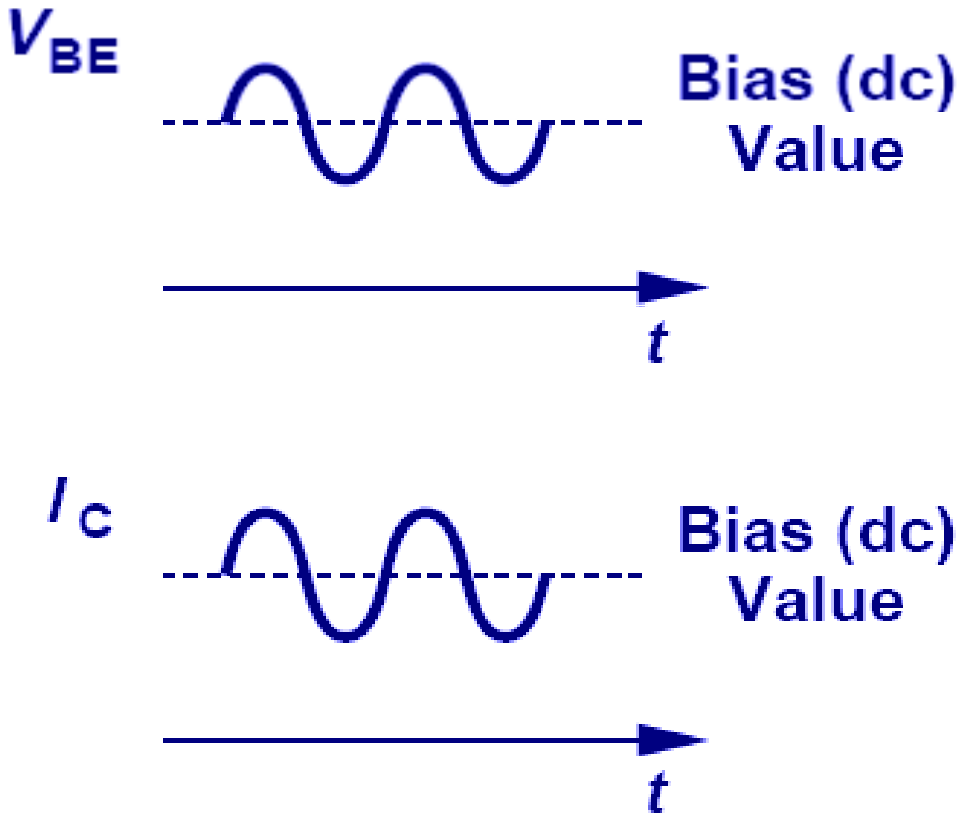


Biasing of BJT

- Transistors and circuits must be biased because

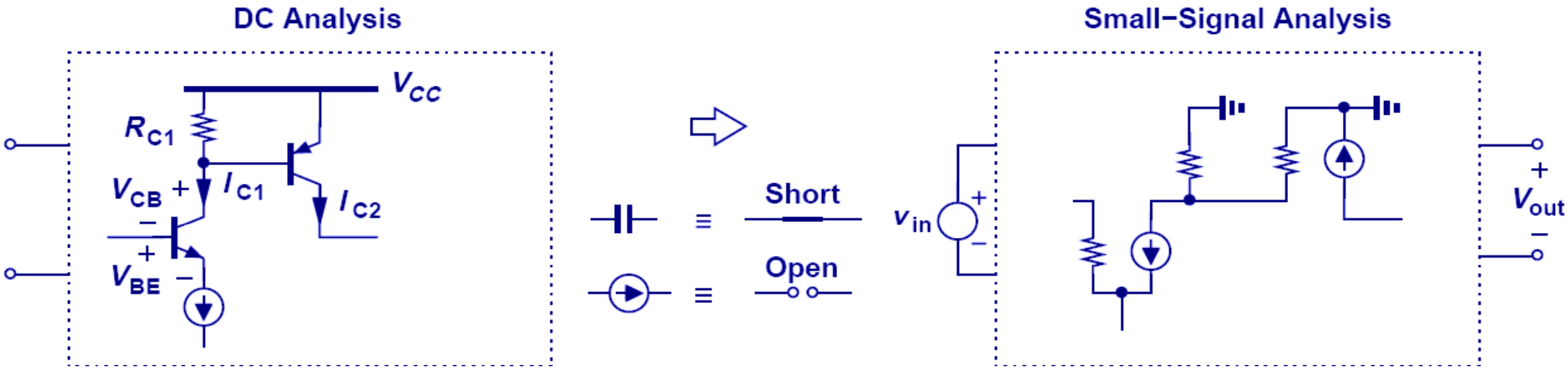
(1) transistors must operate in the active region; the base-emitter and base-collector junctions are forward- and reverse-biased, respectively.

(2) their small-signal parameters depend on the bias conditions; g_m, r_π, r_O depends on I_C.



DC Analysis vs. Small-Signal Analysis

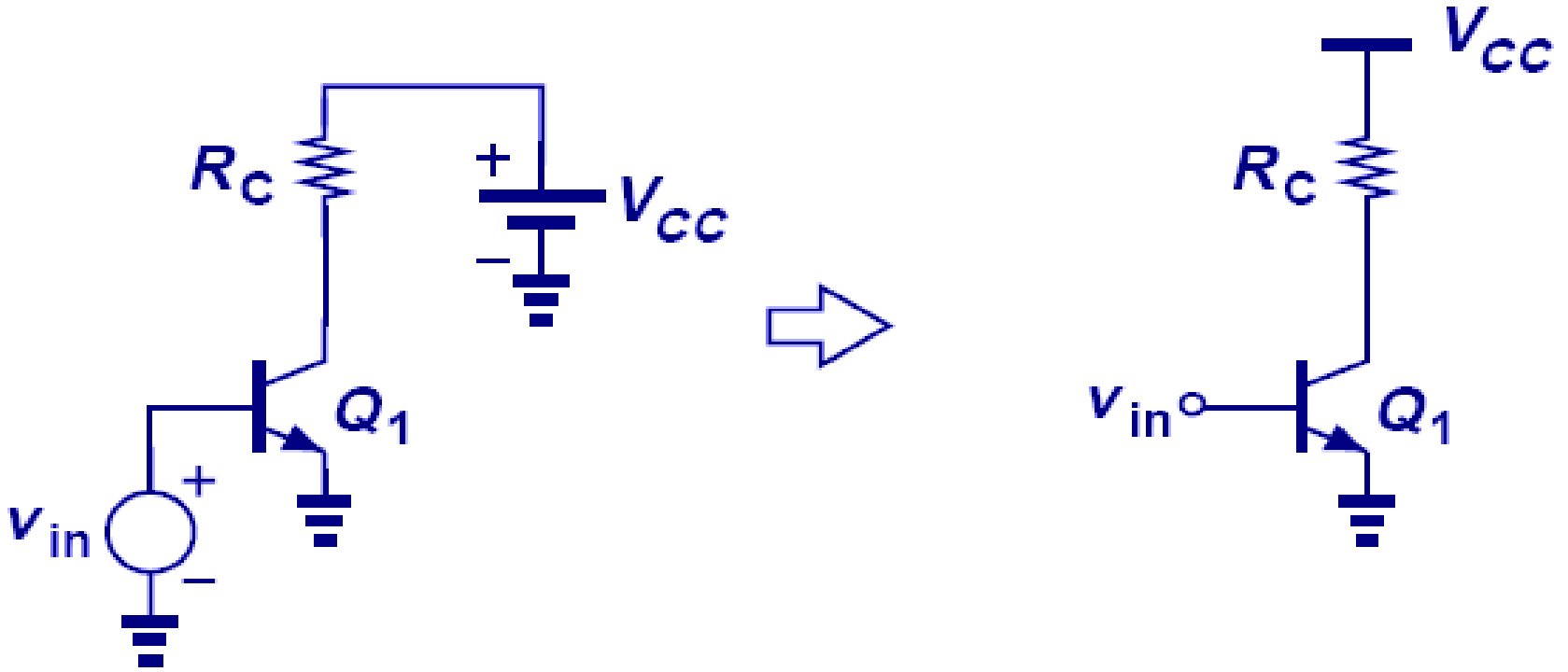
- First, ***DC analysis*** is performed to determine ***operating*** (***quiescent***) ***point*** and obtain small-signal parameters.
- Second, sources are set to zero and small-signal model is used to perform ***small-signal analysis***.
- A rule of thumb, we consider **10%** variation in the collector current as the upper bound for small-signal operation.



Notation Simplification

- Hereafter, the battery that supplies power to the circuit is replaced by a horizontal bar labeled V_{CC}, and input signal is simplified as one node called V_{in}.

  The subscript *CC* indicates supply voltage feeding the collector.



Example 5.5: bad biasing

A student familiar with bipolar devices constructs the circuit shown in Fig. 5.11 and attempts to amplify the signal produced by a microphone. If $I_S = 6\text{x}10^{-16}$ A and the peak value of the microphone signal is 20 mV, determine the peak value of the output signal.

Solution

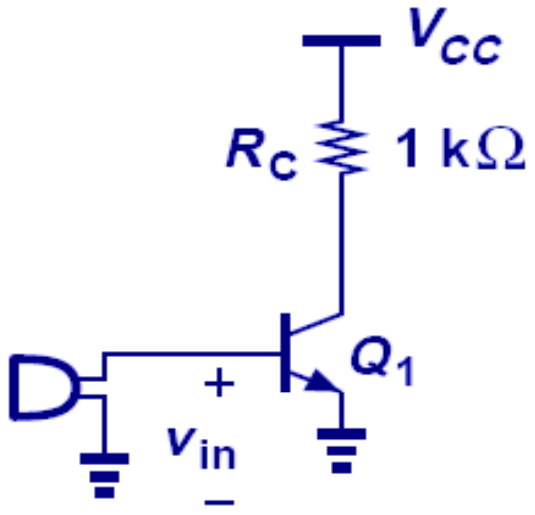
Unfortunately, the student has forgotten to bias the transistor. (The microphone does not produce a dc output). If V_{in} (= V_{BE}) reaches 20 mV, then

$$\Delta I_C = I_S \exp \frac{\Delta V_{BE}}{V_T} = 1.29 \times 10^{-15}\,\text{A}.$$

This change in the collector current yields a change in the output voltage equal to

$$R_C \Delta I_C = 1.29 \times 10^{-12}\,\text{V}.$$

The circuit generates virtually no output because the bias current (in the absence of the microphone signal) is zero and so is the transconductance.



Example 5.6: still bad biasing

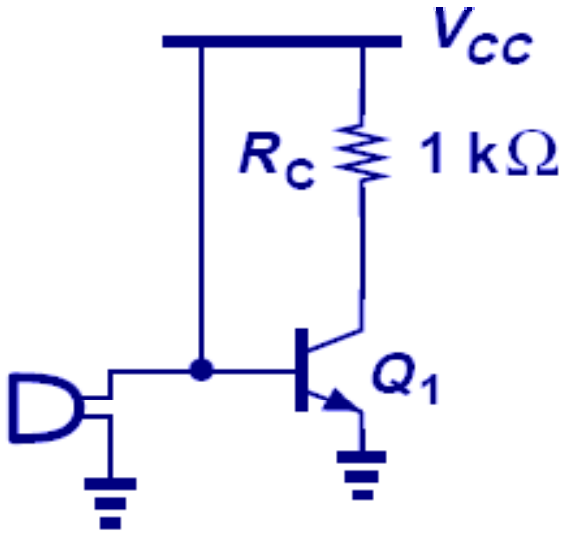
Having realized the bias problem, the student in Example 5.5 modifies the circuit as shown in Fig. 5.12, connecting the base to V_{CC} to allow dc biasing for the base-emitter junction. Explain why the student needs to learn more about biasing.

Solution

The fundamental issue here is that the signal generated by the microphone is *shorted* to V_{CC}. Acting as an ideal voltage source, V_{CC} maintains the base voltage at a *constant* value, prohibiting any change introduced by the microphone. Since V_{BE} remains constant, so does V_{out}, leading to no amplification.

Another important issue relates to the value of V_{BE}: with $V_{BE} = V_{CC} = 2.5\text{V}$, enormous currents flow into the transistor.

check the working region of the transistor



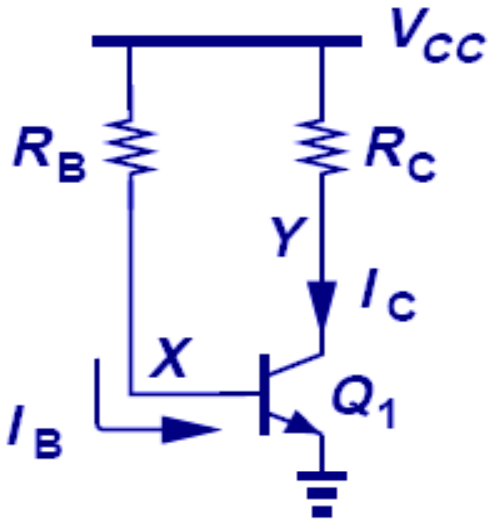
Simple Biasing with Base Resistor

- Base is tied to V_{CC} through a relatively large resistor, R_B, so as to forward-bias the base-emitter junction.
- Assuming a constant value for V_{BE}, about 700 to 800 mV, one can solve for both I_B and I_C and determine the terminal voltages of the transistor.

$$R_B I_B + V_{BE} = V_{CC} \quad \Rightarrow \quad I_B = \frac{V_{CC} - V_{BE}}{R_B}.$$

$$I_C = \beta \frac{V_{CC} - V_{BE}}{R_B},$$

$$V_{CE} = V_{CC} - R_C I_C = V_{CC} - \beta \frac{V_{CC} - V_{BE}}{R_B} R_C.$$



- To avoid saturation completely, the collector voltage must remain above the base voltage:

$$V_{CC} - \beta \frac{V_{CC} - V_{BE}}{R_B} R_C > V_{BE}.$$

- However, bias point is sensitive to β variations, rarely used in practice.

Example 5.7

For the circuit shown in Fig. 5.14, determine the collector bias current. Assume $\beta = 100$ and $I_S = 10^{-17}$ A. Verify that Q_1 operates in the forward active region.

Solution

Since I_S is relatively small, we surmise that the base-emitter voltage required to carry typical current level is relatively large. Thus, we use $V_{BE} = 800$ mV as an initial guess and write Eq. (5.14) as

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \approx 17\,\mu\text{A}.$$

It follows that $I_C = 1.7$ mA.

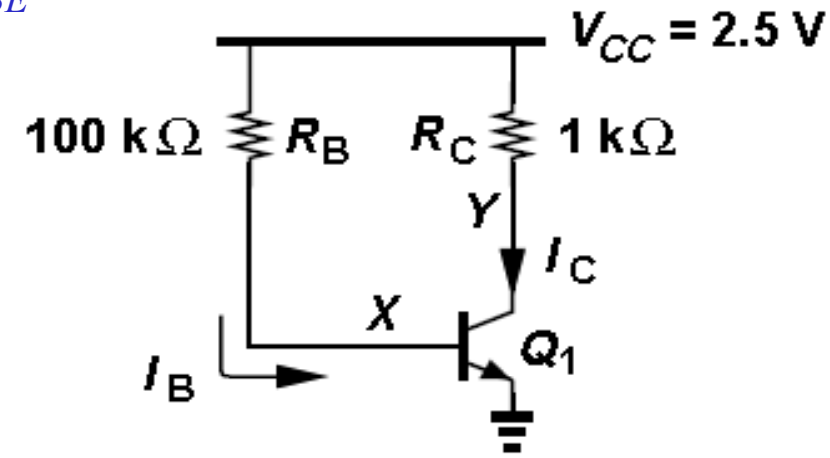
With this result for I_C, we calculate a new value for V_{BE}:

$$V_{BE} = V_T \ln \frac{I_C}{I_S} = 852\,\text{mV},$$

and iterate to obtain more accurate results. That is,

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = 16.5\,\mu\text{A}$$

and hence $I_C = 1.65$ mA



Example 5.7 (cnt'd)

Since the new value of I_C is quite close to initial guess, we consider $I_C = 1.65$ mA accurate enough and iterate no more.

We have

$$V_{CE} = V_{CC} - R_C I_C = 0.85\text{V},$$

a value nearly equal to V_{BE}. The transistor therefore operates near the edge of active and saturation modes.

- The simple biasing is rarely used in practice due to:

  First, the V_{BE} "uncertainty" becomes more severe at low V_{CC} because V_{CC} - V_{BE} determines the base current. Thus, in low-voltage design, the bias is more sensitive to V_{BE} variations among transistors or with temperature.

  Second, I_C heavily depends on β, that may change considerably. In the above example, if β increases from 100 to 120, then I_C rises to 1.98 mA and V_{CE} falls to 0.52, driving the transistor toward heavy saturation.

Improved Biasing: Resistive Divider

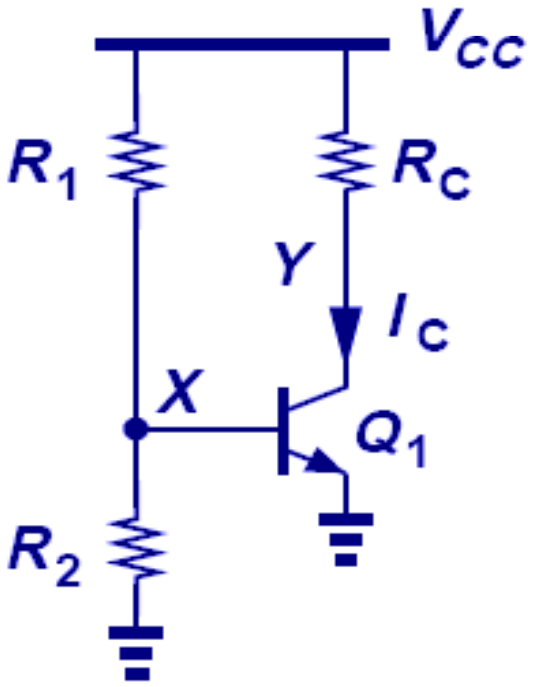
- Using resistor divider to set V_{BE}, it is possible to produce an I_C that is relatively independent of β if base current is small.
- R_1 and R_2 act as a voltage divider, providing a V_{BE} equal to

$$V_X = \frac{R_2}{R_1 + R_2} V_{CC},$$

Thus

$$I_C = I_S \exp\left(\frac{R_2}{R_1 + R_2} \cdot \frac{V_{CC}}{V_T} \right),$$

independent of β.



- Nonetheless, the design must ensure that the base current remains negligible.

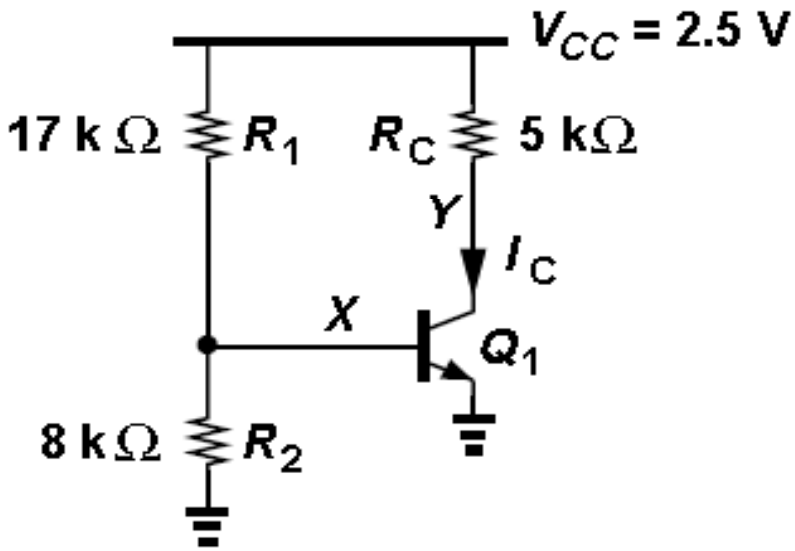
Example 5.8

Determine the collector current of Q_1 in Fig. 5.16 if $I_S = 10^{-17}$ A and $\beta = 100$. Verify that the base current is negligible and the transistor operates in the active mode.

Solution

Neglecting the base current of Q_1, we have

$$V_X = \frac{R_2}{R_1 + R_2} V_{CC} = 800\text{mV}.$$



It follows that

$$I_C = I_S \exp\frac{V_{BE}}{V_T} = 231\mu\text{A}$$

and $I_B = 2.31$ μA.

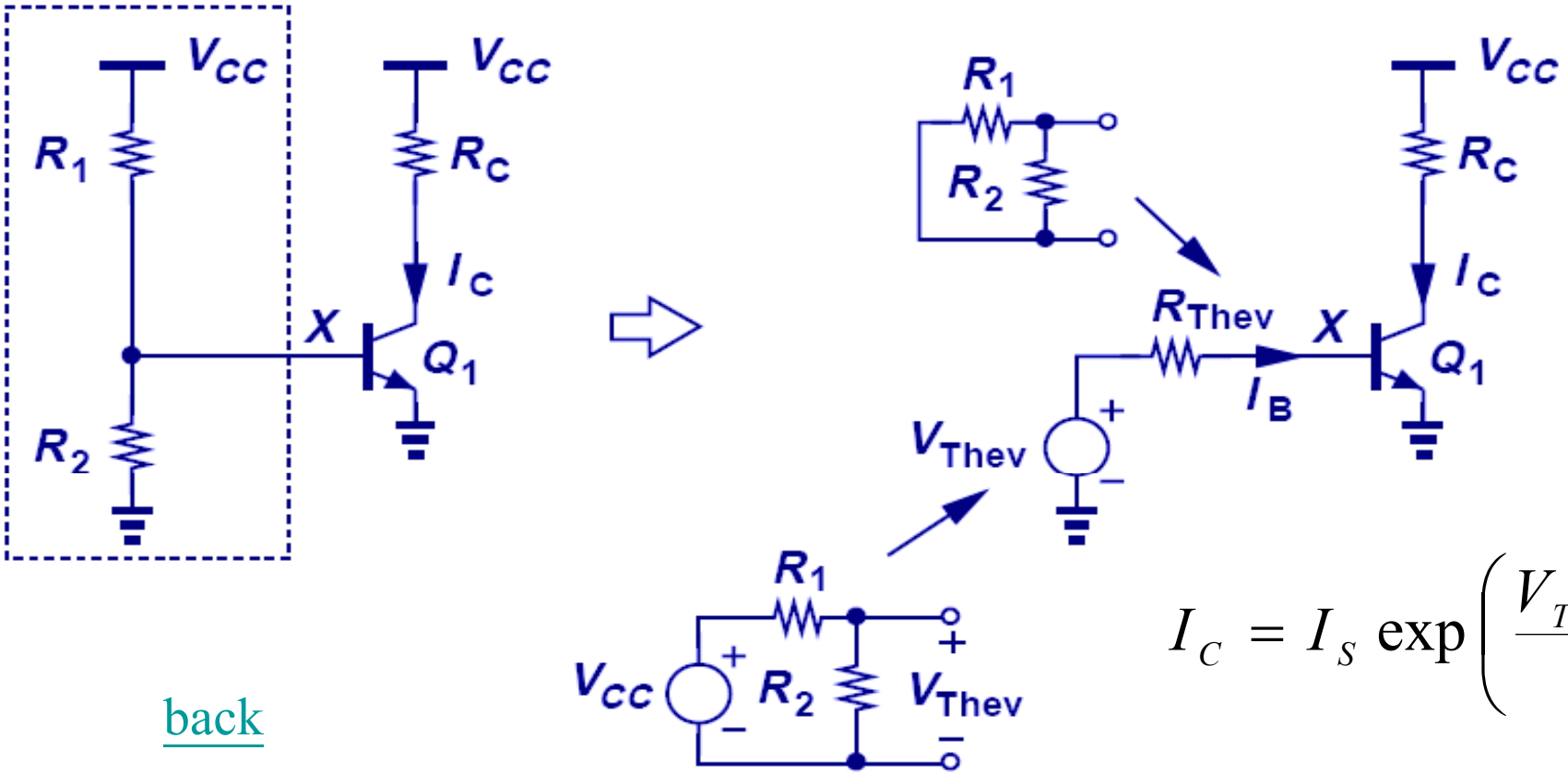
Is the base current negligible? With which quantity should this value be compared? Provided by the resistive divider, I_B must be negligible with respect to the current flowing through R_1 and R_2: $I_B << V_{CC}/(R_1 + R_2)$

This condition indeed holds in this example because $V_{CC}/(R_1 + R_2) = 100$ μA $\approx 43\ I_B$. We also note that $V_{CE} = 1.345$ V, and hence Q_1 operates in the active region.

Accounting for Base Current

- With proper ratio of R_1 and R_2, I_C can be insensitive to β; however, its exponential dependence on resistor deviations makes it less useful.
- If I_B is *not* negligible, replace the voltage divider with a Thevenin equivalent.

$$V_{Thev} = \frac{R_2}{R_1 + R_2} V_{CC}. \qquad R_{Thev} = R_1 \,||\, R_2. \qquad V_X = V_{Thev} - I_B R_{Thev}$$



$$I_C = I_S \exp\left(\frac{V_{Thev} - I_B R_{Thev}}{V_T}\right)$$

back

Example 5.9

Calculate the collector current of Q_1 in Fig. 5.18(a). Assume $\beta = 100$ and $I_S = 10^{-17}$ A.

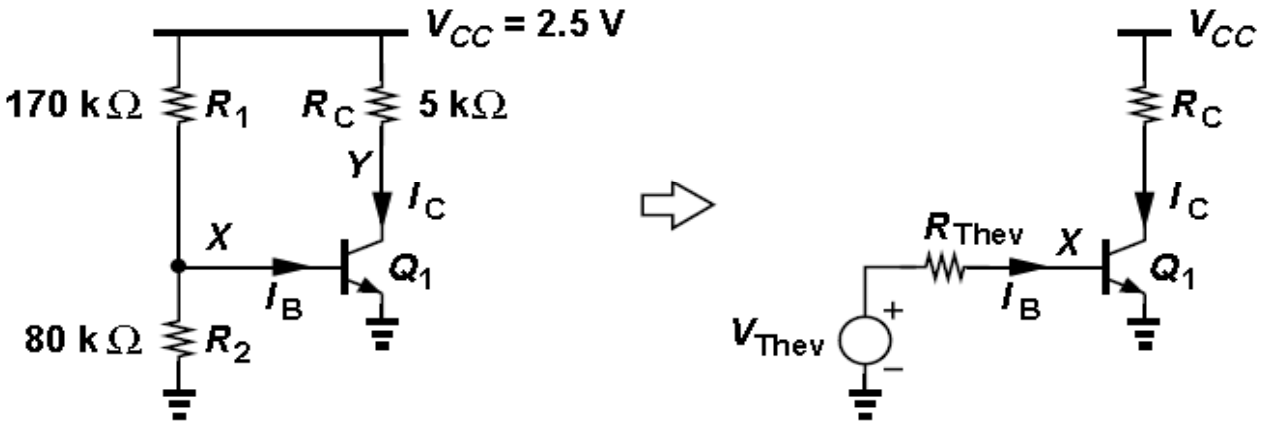
Solution

Constructing the equivalent circuit shown in Fig. 5.18(b), we note that

$$V_{Thev} = \frac{R_2}{R_1 + R_2} V_{CC} = 800\text{mV} \quad \text{and} \quad R_{Thev} = R_1 \parallel R_2 = 54.4\text{k}\Omega.$$

We begin the iteration with an initial guess $V_{BE} = 750$ mV (because we know that the voltage drop across R_{Thev} makes V_{BE} *less* than V_{Thev}), thereby arriving at the base current:

$$I_B = \frac{V_{Thev} - V_{BE}}{R_{Thev}} = 0.919\mu\text{A}.$$



Thus, $I_C = \beta I_B = 91.9$ μA and

$$V_{BE} = V_T \ln \frac{I_C}{I_S} = 776\text{mV}.$$

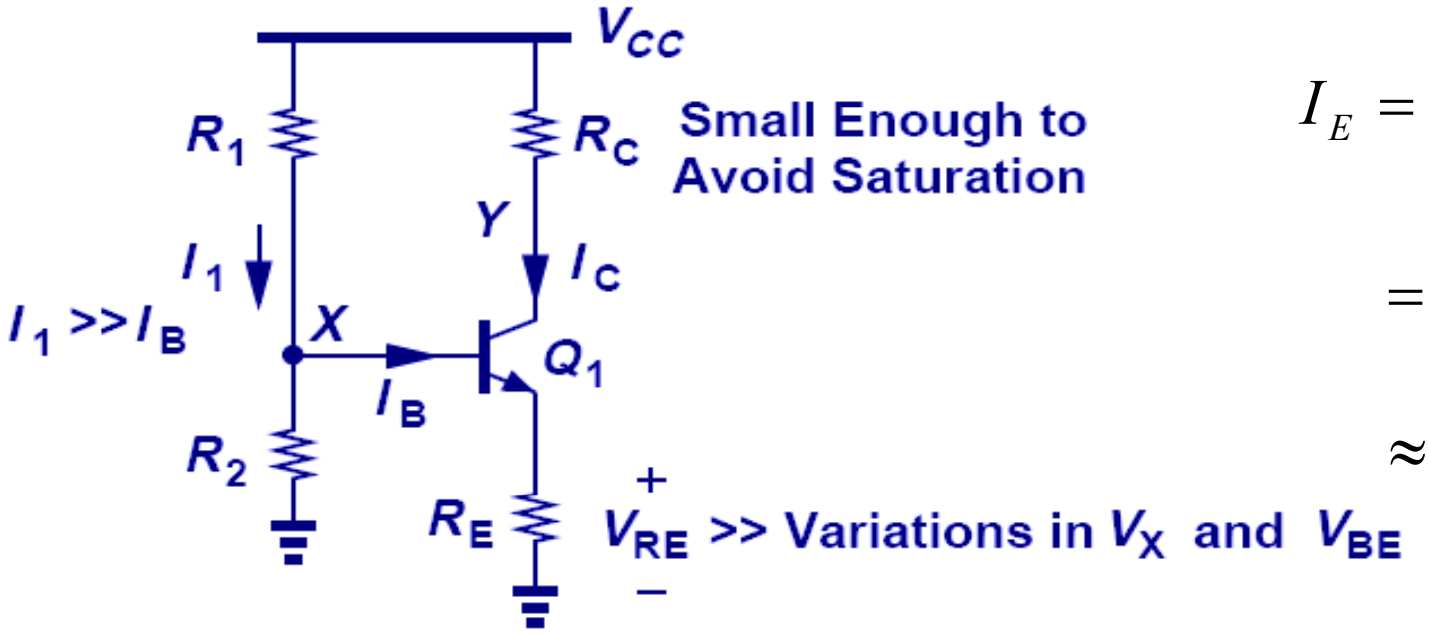
It follows that $I_B = 0.441$ μA and hence $I_C = 44.1$ μA, still a large fluctuation with respect to the first value from above. Continuing the iteration, we obtain $V_{BE} = 757$ mV, $I_B = 0.79$ μA and $I_C = 79.0$ μA. After many iterations, $V_{BE} \approx 766$ mV and $I_C = 63$ μA.

- Proper choice of R_1 and R_2 makes the bias relatively insensitive to β
- The exponential dependence of I_C upon the voltage, V_X, generated by the resistive divider still leads to substantial bias variations.
- For example, if R_2 is 1% higher than its nominal value, so is V_X, thus multiplying the collector current by $\exp(0.01V_{BE}/V_T) \approx 1.36$ (for V_{BE} = 800 mV).
- In other words, a 1% error in one resistor value introduces a 36% error in the collector current.
- The circuit is therefore still of little practical value.

Emitter Degeneration Biasing

- Resistor R_E appears in series with the emitter, thereby lowering the sensitivity to V_{BE}, *i.e.*, R_E helps to absorb the error in V_X so V_{BE} stays relatively constant.
- This bias technique is less sensitive to β ($I_1 >> I_B$) and V_{BE} variations.

$$V_X = V_{CC} R_2/(R_1 + R_2) \qquad V_P = V_X - V_{BE}$$



$$I_E = \frac{V_P}{R_E}$$

$$= \frac{1}{R_E}\left(V_{CC}\frac{R_2}{R_1 + R_2} - V_{BE}\right)$$

$$\approx I_C,$$

(1) $I_1 >> I_B$ to lower sensitivity to β, and

(2) V_{RE} must be large enough (100 mV to several hundred mV) to suppress the effect of uncertainties in V_X and V_{BE}.

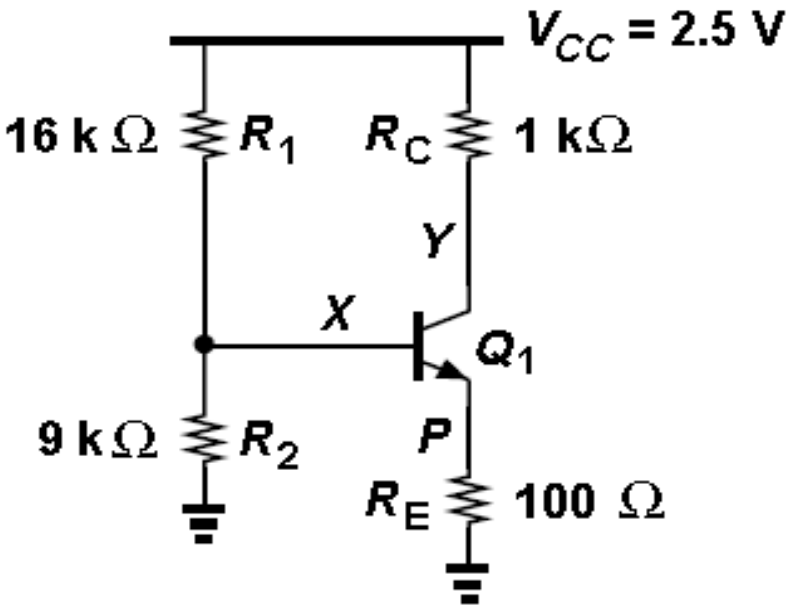
Example 5.10

Calculate the bias currents in the circuit of Fig. 5.20 and verify that Q_1 operates in the forward active region. Assume β =100 and $I_S = 5\text{x}10^{-17}$ A. How much does the collector current change if R_2 is 1% higher than its nominal value?

Solution

We neglect the base current and write

$$V_X = V_{CC}\frac{R_2}{R_1 + R_2} = 900\text{mV}.$$



Using V_{BE} = 800 mV as an initial guess, we have

$$V_P = V_X - V_{BE} = 100\text{ mV}.$$

and hence $I_C \approx I_E \approx 1$ mA.

With this result, we must reexamine the assumption of V_{BE} = 800 mV. Since

$$V_{BE} = V_T \ln\frac{I_C}{I_S} = 796\text{mV},$$

we conclude that the initial guess is reasonable. Furthermore, Eq. (5.57) suggests that a 4-mV error in V_{BE} leads to a 4% error in V_P and hence I_E, indicating a good approximation.

Example 5.10 (cnt'd)

Let us now determine if Q_1 operates in the active mode. The collector voltage is given by

$$V_Y = V_{CC} - I_C R_C = 1.5\text{V}.$$

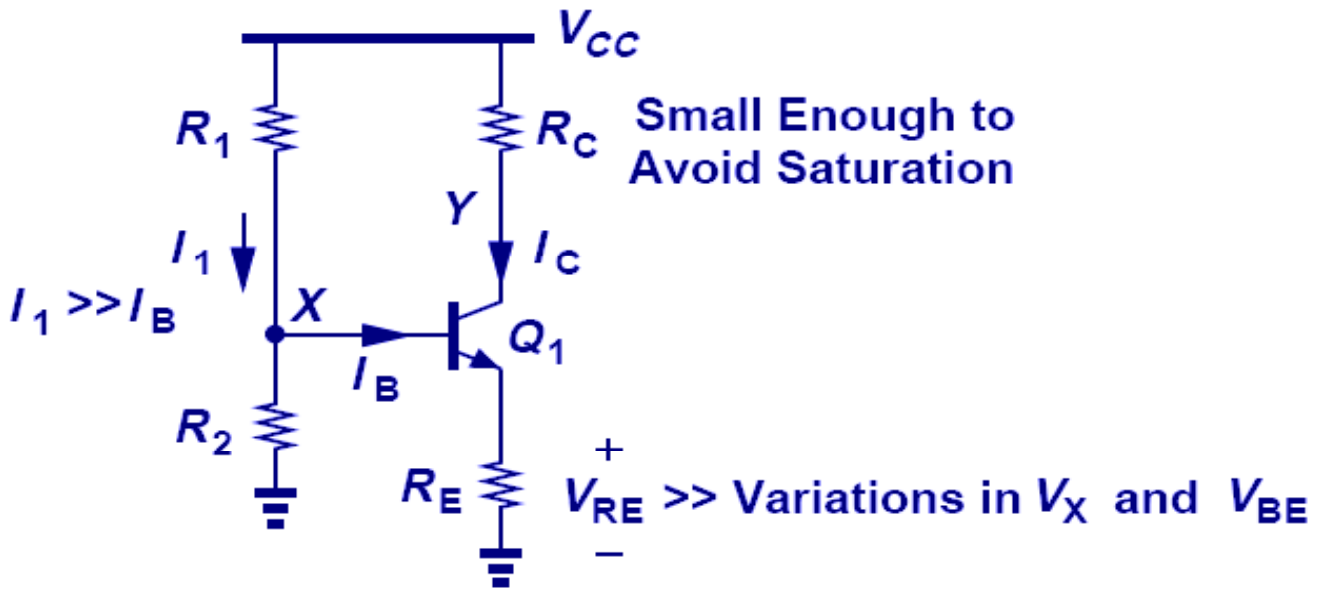
With the base voltage at 0.9 V, the device is indeed in the active region.

Is the assumption of negligible base current valid? With $I_C \approx 1$ mA, $I_B \approx 10$ μA whereas the current flowing through R_1 and R_2 is equal to 100 μA. The assumption is therefore reasonable. For greater accuracy, an iterative procedure similar to that in Example 5.9 can be followed.

If R_2 is 1% higher than its nominal value, then (5.54) indicates that V_X rises to approximately 909 mV. We may assume that the 9-mV change directly appears across R_E, raising the emitter current by 9mV/100Ω = 90 μA. From Eq. (5.56), we note that this assumption is equivalent to considering V_{BE} constant, which is reasonable because the emitter and collector currents have changed by only 9%.

Design Procedure

1. Choose an I_C to provide the necessary small signal parameters, g_m, r_π, etc.
2. Considering the variations of R_1, R_2, and V_{BE}, choose a value for $V_{RE} \approx I_C R_E$.
3. With V_{RE} chosen, and $V_{BE} = V_T \ln(I_C/I_S)$ calculated, $V_x = V_{BE} + V_{RE}$ can be determined.
4. Select R_1 and R_2 to provide V_x.
5. Determined by small-signal gain requirements, the value of R_C is bounded by a maximum that places Q_1 at the edge of saturation.



Example 5.11

Design the circuit of Fig. 5.21 so as to provide a transconductance of 1/52Ω for Q_1. Assume $V_{CC} = 2.5$ V, $\beta = 100$, and $I_S = 5\text{x}10^{-17}$ A. What is the maximum tolerable value of R_C?

Solution

A g_m of $(52\Omega)^{-1}$ translates to a collector current of 0.5 mA and a V_{BE} of 778 mV. Assuming $R_E I_C = 200$ mV, we obtain $R_E = 400\ \Omega$. To establish $V_x = V_{BE} + R_E I_C = 978$ mV, we must have

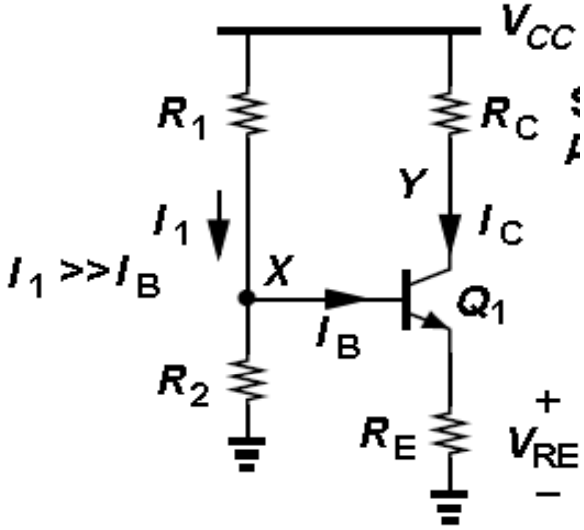
$$\frac{R_2}{R_1 + R_2} V_{CC} = V_{BE} + R_E I_C,$$

where the base current is neglected. For the base current $I_B = 5\ \mu$A to be negligible,

$$\frac{V_{CC}}{R_1 + R_2} >> I_B$$

e.g., by a factor of 10. Thus, $R_1 + R_2 = 50$ kΩ, which in conjunction with (5.63) yields

$R_1 = 30.45$ kΩ, and $R_2 = 19.55$ kΩ.



Example 5.11 (cnt'd)

How large can R_C be? Since the collector voltage is equal to V_{CC} - $R_C I_C$, we pose the following constraint to ensure active mode operation:

$$V_{CC} - R_C I_C > V_X;$$

that is,

$$R_C I_C < 1.522\text{V}.$$

Consequently,

$$R_C < 3.044\text{k}\Omega.$$

If R_C exceeds this value, the collector voltage falls below the base voltage. As mentioned in Chapter 4, the transistor can tolerate soft saturation, i.e., up to about 400 mV of base-collector forward bias. Thus, in low-voltage applications, we may allow $V_Y \approx V_X$ - 400 mV and hence a greater value for R_C.

Design Trade-Offs

- Specifically, an overly conservative design faces the following issues:

(1) if we wish I_1 to be much much greater than I_B, then $R_1 + R_2$ and hence R_1 and R_2 are quite small, leading to a low *input impedance*;

(2) if we choose a very large V_{RE}, then V_X (= $V_{BE} + V_{RE}$) must be high, thereby limiting the minimum value of the collector voltage to avoid saturation.

Example 5.12

Repeat Example 5.11 but assuming $V_{RE} = 500$ mV and $I_1 \geqq 100\, I_B$.

Solution

The collector current and base-emitter voltage remain unchanged. The value of R_E is now given by 500mV/0.5mA = 1 kΩ. Also, $V_X = V_{BE} + I_C R_E = 1.278$ V and (5.63) still holds. We rewrite (5.64) as

$$\frac{V_{CC}}{R_1 + R_2} \geq 100 I_B,$$

obtaining $R_1 + R_2 = 5$ kΩ. It follows that $R_1 = 1.45$ kΩ, and $R_2 = 3.55$ kΩ.

Since the base voltage has risen to 1.278 V, the collector voltage must exceed this value to avoid saturation, leading to

$$R_C < \frac{V_{CC} - V_X}{I_C} < 1.044\text{k}\Omega.$$

As seen in Section 5.3.1, the reduction in R_C translates to a lower voltage gain. Also, the much smaller values of R_1 and R_2 here than in Example 5.11 introduce a low input impedance, loading the preceding stage. We compute the exact input impedance of this circuit in Section 5.3.1.

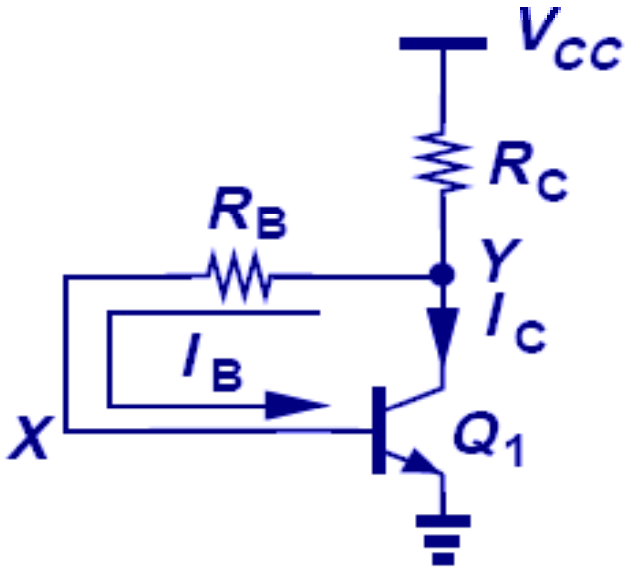
Self-Biasing Technique

- This bias technique utilizes the collector voltage to provide the necessary V_x and I_B.
- One important characteristic of this technique is that collector has a higher potential than the base, thus guaranteeing active operation of the transistor. $V_X = V_Y - I_B R_B$.
- Assuming $I_B << I_C$, yield $V_Y = V_{CC} - I_C R_C$
- Also

$$V_Y = R_B I_B + V_{BE} = \frac{R_B I_C}{\beta} + V_{BE}.$$

- Gives

$$I_C = \frac{V_{CC} - V_{BE}}{R_C + \frac{R_B}{\beta}}.$$



- As usual, we begin with an initial guess for V_{BE}, compute I_C, and utilize $V_{BE} = V_T \ln (I_C/I_S)$ to improve the accuracy of our calculations.

Example 5.13

Determine the collector current and voltage of Q_1 in Fig. 5.22 if $R_C = 1$ kΩ, $R_B = 10$ kΩ, $V_{CC} = 2.5$ V, $I_S = 5\text{x}10^{-17}$ A, and β = 100. Repeat the calculations for $R_C = 2$ kΩ.

Solution

Assuming $V_{BE} = 0.8$ V, we have from (5.78):

$$I_C = \frac{V_{CC} - V_{BE}}{R_C + \dfrac{R_B}{\beta}}.$$

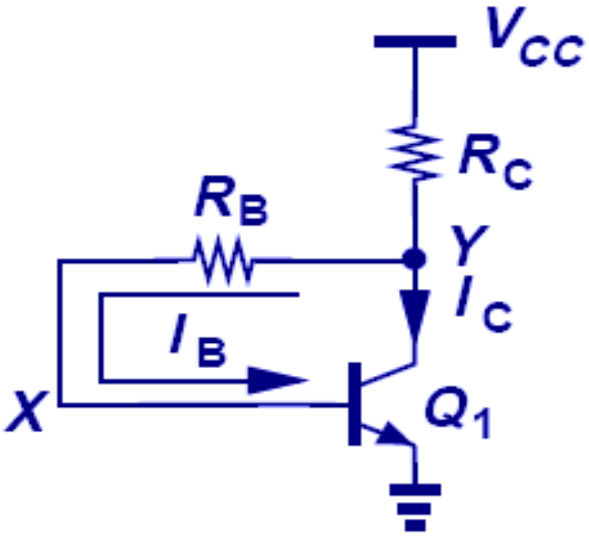
$$I_C = 1.545 \text{ mA}$$

and hence $V_{BE} = V_T \ln (I_C/I_S) = 807.6$ mV, concluding that the initial guess for V_{BE} and the value of I_C given by it are reasonably accurate. We also note that $R_B I_B = 154.5$ mV and $V_Y = R_B I_B + V_{BE} \approx 0.955$ V.

If $R_C = 2$ kΩ, then with $V_{BE} = 0.8$ V, Eq. (5.78) gives

$$I_C = 0.810 \text{ mA}$$

To check the validity of the initial guess, we write $V_{BE} = V_T \ln (I_C/I_S) = 791$ mV. Compared with V_{CC} - V_{BE} in the numerator of (5.78), the 9-mV error is negligible and the value of I_C in (5.80) is acceptable. Since $R_B I_B = 81$ mV, $V_Y \approx 0.881$ V.



Self-Biasing Design Guidelines

- Two important guidelines for the self-biased stage:

  (1) V_{CC} - V_{BE} must be much greater than the uncertainties in the value of V_{BE};

  (2) R_C must be much greater than R_B/β to lower sensitivity to β.

- In fact, if $R_C >> R_B/\beta$, then $$I_C \approx \frac{V_{CC} - V_{BE}}{R_C},$$

- **Design Procedure**

  With the required value of I_C known from small-signal considerations, choose $R_C = 10\, R_B/\beta$ and rewrite (5.78) as

$$I_C = \frac{V_{CC} - V_{BE}}{1.1 R_C},$$

  That is,

$$R_C = \frac{V_{CC} - V_{BE}}{1.1 I_C} \qquad R_B = \frac{\beta R_C}{10}.$$

  The choice of R_B also depends on small-signal requirements and may deviate from this value, but it must remain substantially lower than βR_C.

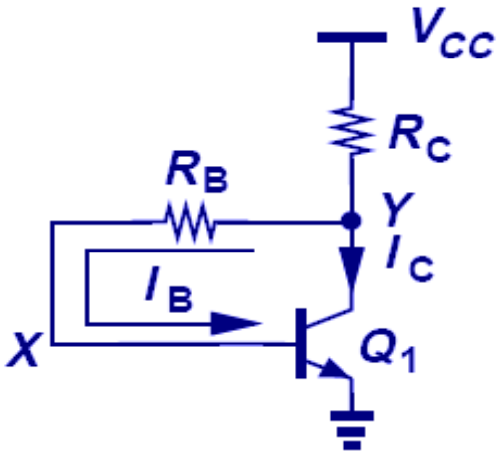
Example 5.14

Design the self-biased stage of Fig. 5.22 for $g_m = 1/13\Omega$ and $V_{CC} = 1.8$ V. Assume $I_S = 5\text{x}10^{-16}$ A and $\beta = 100$.

Solution

Since $g_m = I_C/V_T = 1/13\Omega$, we have $I_C = 2$ mA, $V_{BE} = 754$ mV, and

$$R_C \approx \frac{V_{CC} - V_{BE}}{1.1 I_C} \approx 475\Omega.$$

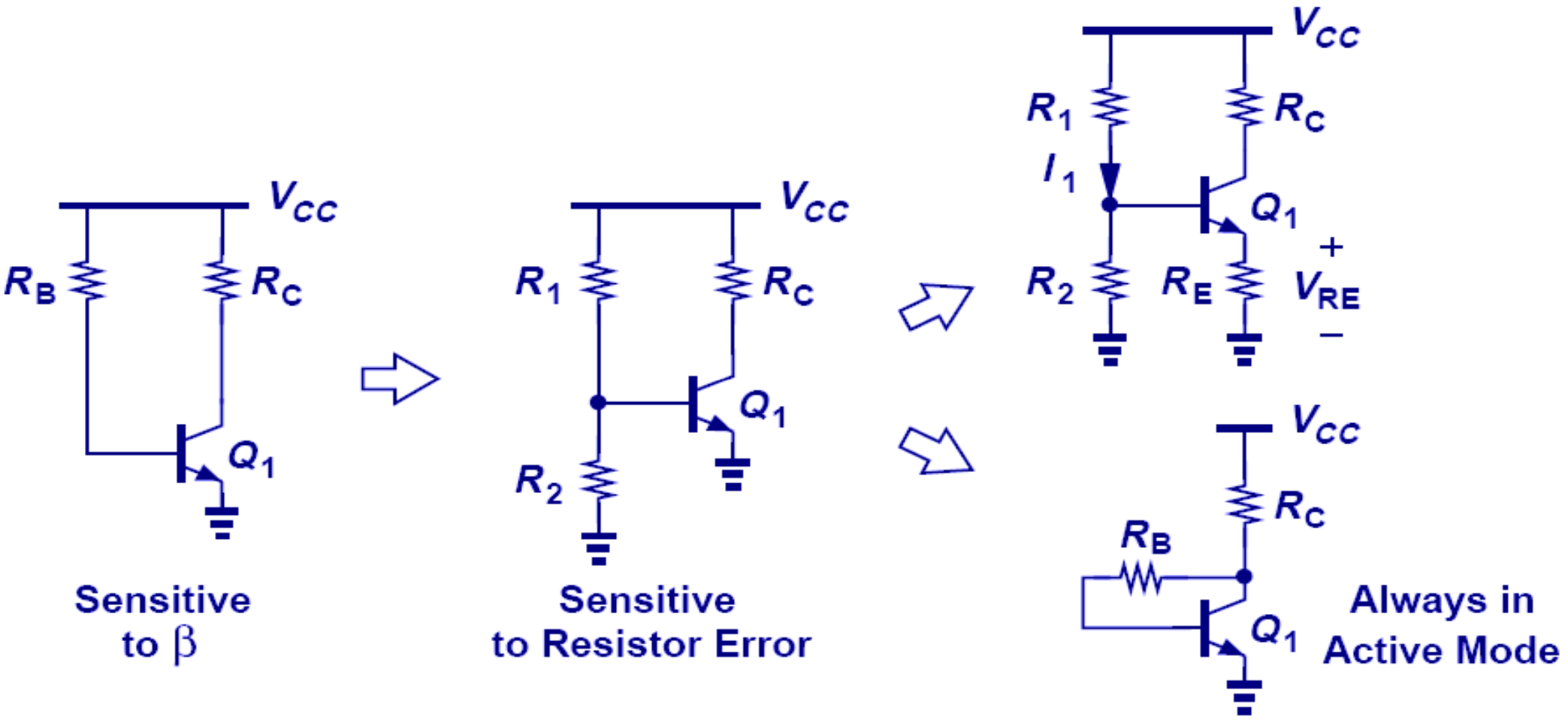


Also,

$$R_B = \frac{\beta R_C}{10} = 4.75\text{k}\Omega.$$

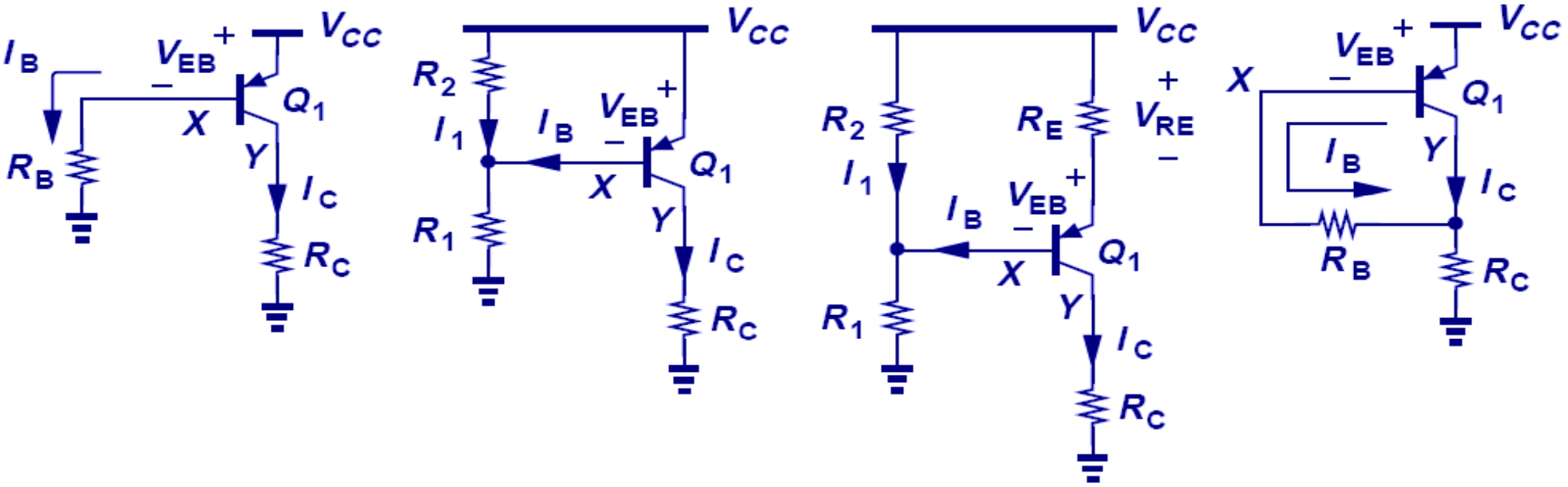
Note that $R_B I_B = 95$ mV, yielding a collector voltage of 754 + 95 = 849 mV.

Summary of Biasing Techniques



PNP Biasing Techniques

- Same principles that apply to NPN biasing also apply to PNP biasing with only polarity modifications.



Example 5.15

Calculate the collector and voltage of Q_1 in the circuit of Fig. 5.24 and determine the maximum allowable value of R_C for operation in the active mode.

Solution

The topology is the same as that in Fig. 5.13 and we have,

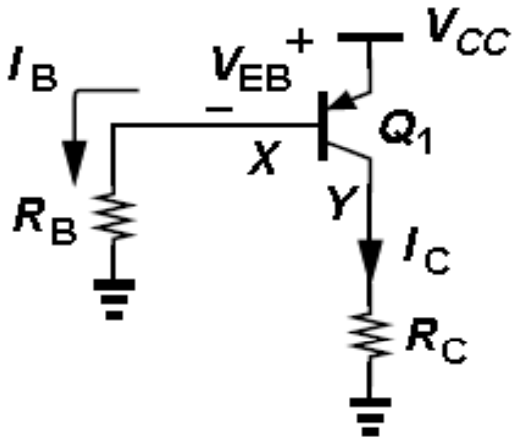
$$I_B R_B + V_{EB} = V_{CC}.$$

That is,

$$I_B = \frac{V_{CC} - V_{EB}}{R_B}$$

and

$$I_C = \beta \frac{V_{CC} - V_{EB}}{R_B}.$$



The circuit suffers from sensitivity to β.

Example 5.15 (cnt'd)

If R_C is increased, V_Y rises, thus approaching V_X (= V_{CC} - V_{EB}) and bringing Q_1 closer to saturation. The transistor enters saturation at $V_Y = V_X$, i.e.,

$$I_C R_{C,max} = V_{CC} - V_{EB}$$

and hence

$$R_{C,max} = \frac{V_{CC} - V_{EB}}{I_C} = \frac{R_B}{\beta}.$$

From another perspective, since $V_X = I_B R_B$ and $V_Y = I_C R_C$, we have $I_B R_B = I_C R_{C,max}$ as the condition for edge of saturation, obtaining $R_B = \beta R_{C,max}$.

Example 5.16

Determine the collector current and voltage of Q_1 in the circuit of Fig. 5.25(a).

Solution

As a general case, we assume I_B is significant and construct the Thevenin equivalent of the voltage divider as depicted in Fig. 5.25(b):

$$V_{Thev} = \frac{R_1}{R_1 + R_2} V_{CC} \qquad R_{Thev} = R_1 \,||\, R_2 .$$

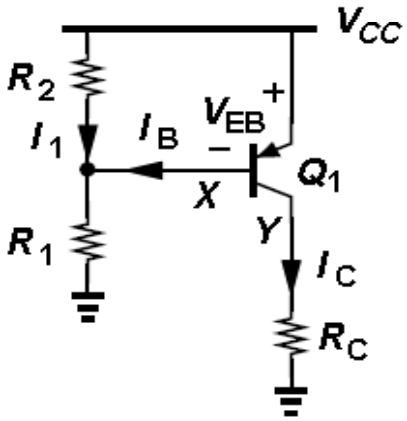
Adding the voltage drop across R_{Thev} and V_{EB} to V_{Thev} yields

$$V_{Thev} + I_B R_{Thev} + V_{EB} = V_{CC};$$

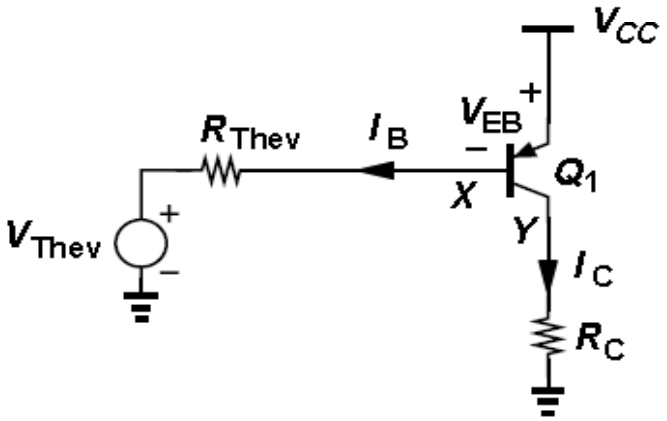
that is,

$$I_B = \frac{V_{CC} - V_{Thev} - V_{EB}}{R_{Thev}}$$

$$= \frac{\dfrac{R_2}{R_1 + R_2} V_{CC} - V_{EB}}{R_{Thev}}.$$



(a)



(b)

Example 5.16 (cnt'd)

It follows that

$$I_C = \beta \frac{\frac{R_2}{R_1 + R_2} V_{CC} - V_{EB}}{R_{Thev}}.$$

As in Example 5.9, some iteration between I_C and V_{EB} may be necessary.

Equation (5.100) indicates that if I_B is significant, then the transistor bias heavily depends on β. On the other hand, if $I_B << I_1$, we equate the voltage drop across R_2 to V_{EB}, thereby obtaining the collector current:

$$\frac{R_2}{R_1 + R_2} V_{CC} = V_{EB}$$

$$I_C = I_S \exp\left(\frac{R_2}{R_1 + R_2} \frac{V_{CC}}{V_T} \right).$$

Note that this result is identical to Eq. (5.30).

Example 5.17

Assuming a negligible base current, calculate the collector current and voltage of Q_1 in the circuit of Fig. 5.26. What is the maximum allowable value of R_C for Q_1 to operate in the forward active region?

Solution

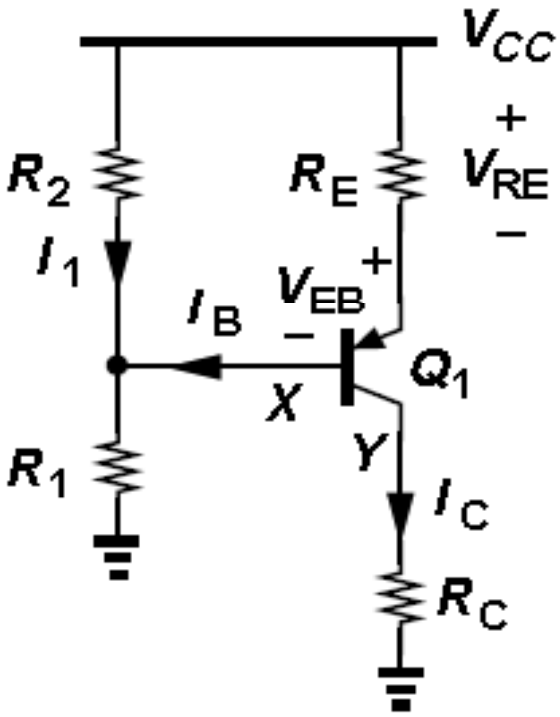
With $I_B << I_1$, we have $V_X = V_{CC}R_1/(R_1+R_2)$. Adding to V_X the emitter-base voltage and the drop across R_E, we obtain

$$V_X + V_{EB} + R_E I_E = V_{CC}$$

and hence

$$I_E = \frac{1}{R_E}\left(\frac{R_2}{R_1 + R_2}V_{CC} - V_{EB}\right).$$

Using $I_C \approx I_E$, we can compute a new value for V_{EB} and iterate if necessary. Also, with $I_B = I_C/\beta$, we can verify the assumption $I_B << I_1$.



Example 5.17 (cnt'd)

In arriving at (5.104), we have written a KVL from V_{CC} to ground, Eq. (5.103). But a more straightforward approach is to recognize that the voltage drop across R_2 is equal to $V_{EB} + I_E R_E$, i.e.,

$$V_{CC}\frac{R_2}{R_1+R_2} = V_{EB} + I_E R_E, \qquad (105)$$

which yields the same result as in (5.104).

The maximum allowable value of R_C is obtained by equating the base and collector voltages:

$$V_{CC}\frac{R_1}{R_1+R_2} = R_{C,max} I_C \qquad (106)$$

$$\approx \frac{R_{C,max}}{R_E}\left(\frac{R_2}{R_1+R_2}V_{CC} - V_{EB}\right). \qquad (107)$$

It follows that

$$R_{C,max} = R_E V_{CC}\frac{R_1}{R_1+R_2}\cdot\frac{1}{\frac{R_2}{R_1+R_2}V_{CC} - V_{EB}}. \qquad (108)$$

Example 5.18

Determine the collector current and voltage of Q_1 in the self-biased circuit of Fig. 5.27.

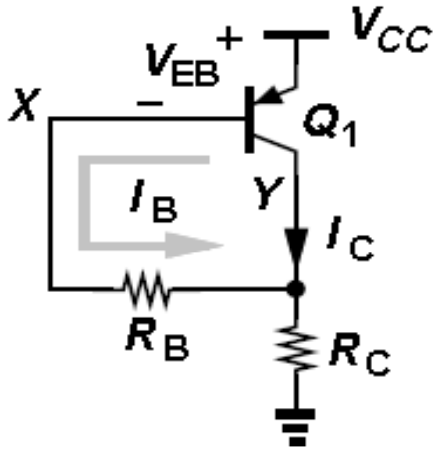
Solution

We must write a KVL from V_{CC} through the emitter-base junction of Q_1, R_B, and R_C to ground. Since $\beta >> 1$ and hence $I_B << I_C$, R_C carries a current approximately equal to I_C, creating $V_Y = I_C R_C$. Moreover, $V_X = I_B R_B + V_Y = I_B R_B + I_C R_C$, yielding

$$V_{CC} = V_{EB} + V_X \tag{109}$$

$$= V_{EB} + R_B I_B + I_C R_C \tag{110}$$

$$= V_{EB} + \left(\frac{R_B}{\beta} + R_C \right) I_C . \tag{111}$$



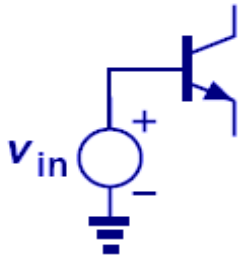
Thus,

$$I_C = \frac{V_{CC} - V_{EB}}{\dfrac{R_B}{\beta} + R_C}, \tag{112}$$

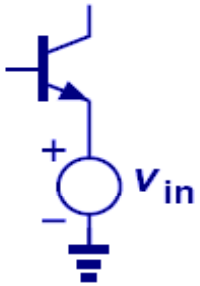
a result similar to Eq. (5.78). As usual, we begin with a guess for V_{EB}, compute I_C, and determine a new value for V_{EB}, etc. Note that, since the base is *higher* than the collector voltage, Q_1 always remains in the active mode.

Possible Bipolar Amplifier Topologies

- Three possible ways to apply an input to an amplifier and three possible ways to sense its output.
- However, in reality only three of six input/output combinations are useful.



(a)



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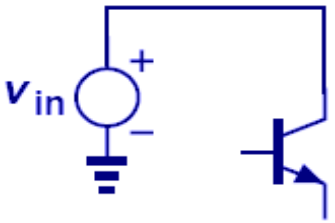

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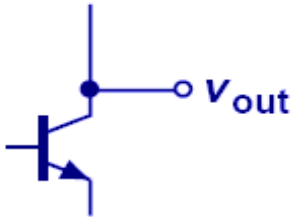

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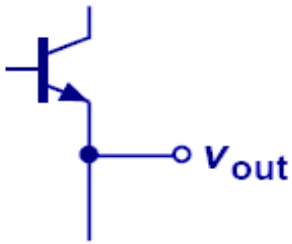

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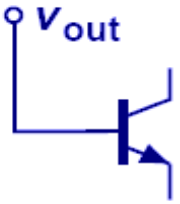
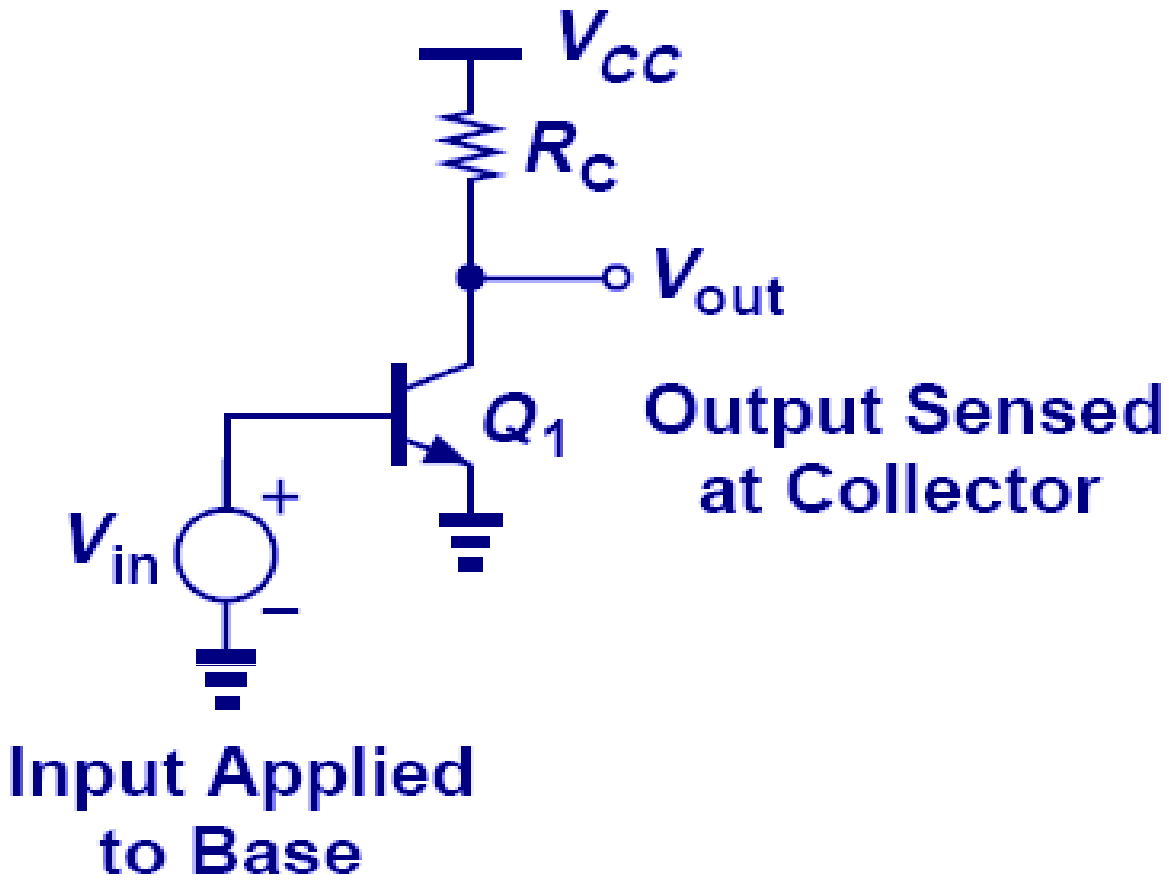


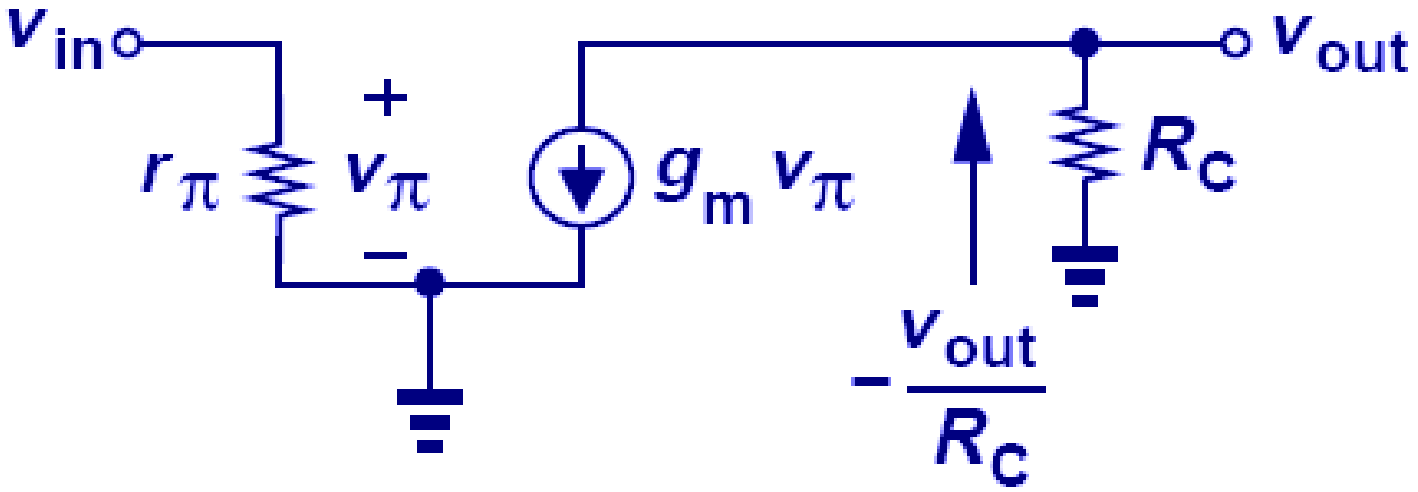
(f)

Common-Emitter Topology

- Input is applied to the base and the output is sensed at the collector.
- The emitter terminal is grounded and hence appears *in common* to the input and output ports.



Small Signal of CE Amplifier



$$A_v = \frac{v_{out}}{v_{in}}$$

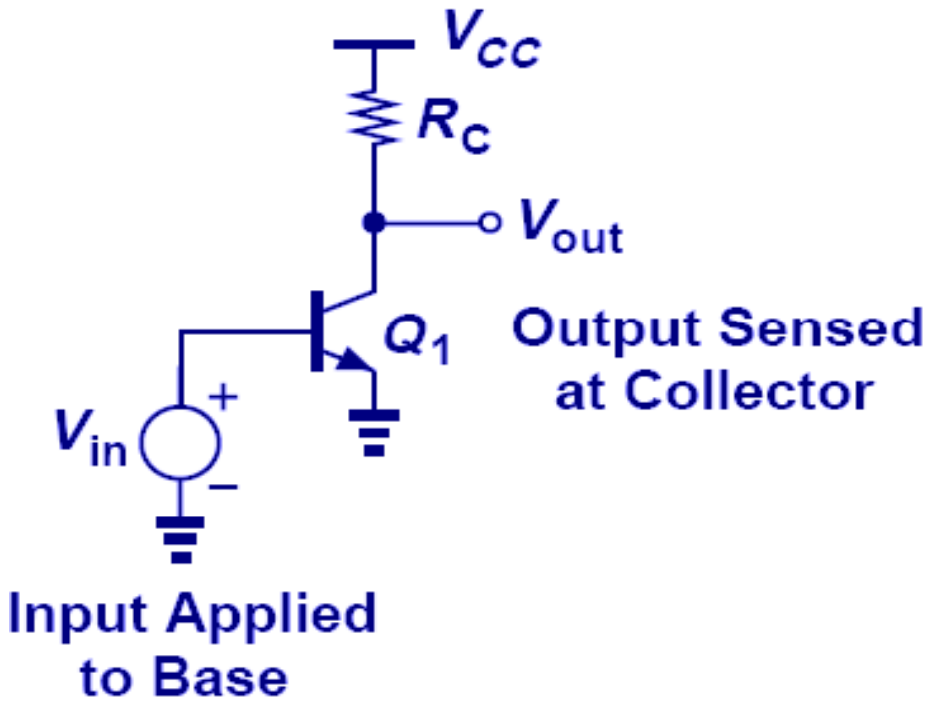
$$-\frac{v_{out}}{R_C} = g_m v_\pi = g_m v_{in}$$

$$A_v = -g_m R_C$$

- Neglect the Early effect now
- The small-signal gain, A_v, is negative because raising the base voltage and hence the collector current lowers v_{out}.
- A_v is proportional to g_m (i.e., the collector bias current) and the collector resistor, R_C.

Limitation on CE Voltage Gain

- Since g_m can be written as I_C/V_T, the CE voltage gain can be written as the ratio of V_{RC} and V_T.
- V_{RC} is the potential difference between V_{CC} and V_{CE}, and V_{CE} cannot go below V_{BE} in order for the transistor to be in active region.



$$|A_v| = \frac{I_C R_C}{V_T}$$

$$|A_v| = \frac{V_{RC}}{V_T}$$

$$|A_v| < \frac{V_{CC} - V_{BE}}{V_T}$$

Example 5.19

Design a CE core with $V_{CC} = 1.8$ V and a power budget, P, of 1 mW while achieving maximum voltage gain.

Solution

Since $P = I_C V_{CC} = 1$ mW, we have $I_C = 0.556$ mA. The value of R_C that places Q_1 at the edge of saturation is given by

$$V_{CC} - R_C I_C = V_{BE}, \qquad (119)$$

which, along with $V_{BE} \approx 800$ mV, yields

$$R_C \leq \frac{V_{CC} - V_{BE}}{I_C} = 1.8\ \text{k}\Omega \qquad (120)\ (121)$$

The voltage gain is therefore equal to

$A_V < (1.8 - 0.8)/26\text{m} = 38.5$

$$A_v = -g_m R_C = -38.5. \qquad (122)(123)$$

Under this condition, an input signal drives the transistor into saturation. As illustrated in Fig. 5.31(a), a 2-mV_{pp} input results in a 77-mV_{pp} output, forward-biasing the base-collector junction for half of each cycle. Nevertheless, so long as Q_1 remains in soft saturation ($V_{BC} > 400$ mV), the circuit amplifies properly.

Example 5.19 (cnt'd)

A more aggressive design may allow Q_1 to operate in soft saturation, e.g., $V_{CE} \approx 400$ mV and hence

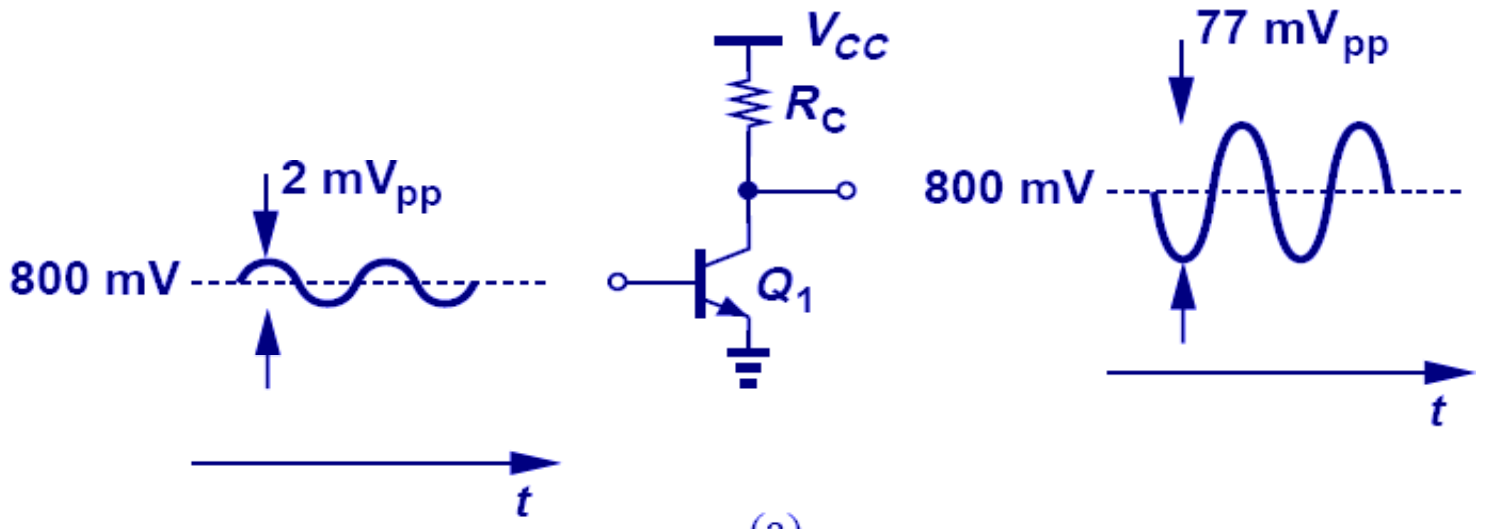
$$R_C \leq \frac{V_{CC} - 400\text{mV}}{I_C} = 2.52\ \text{k}\Omega \qquad (124)(125)$$

In this case, the maximum voltage gain is given by

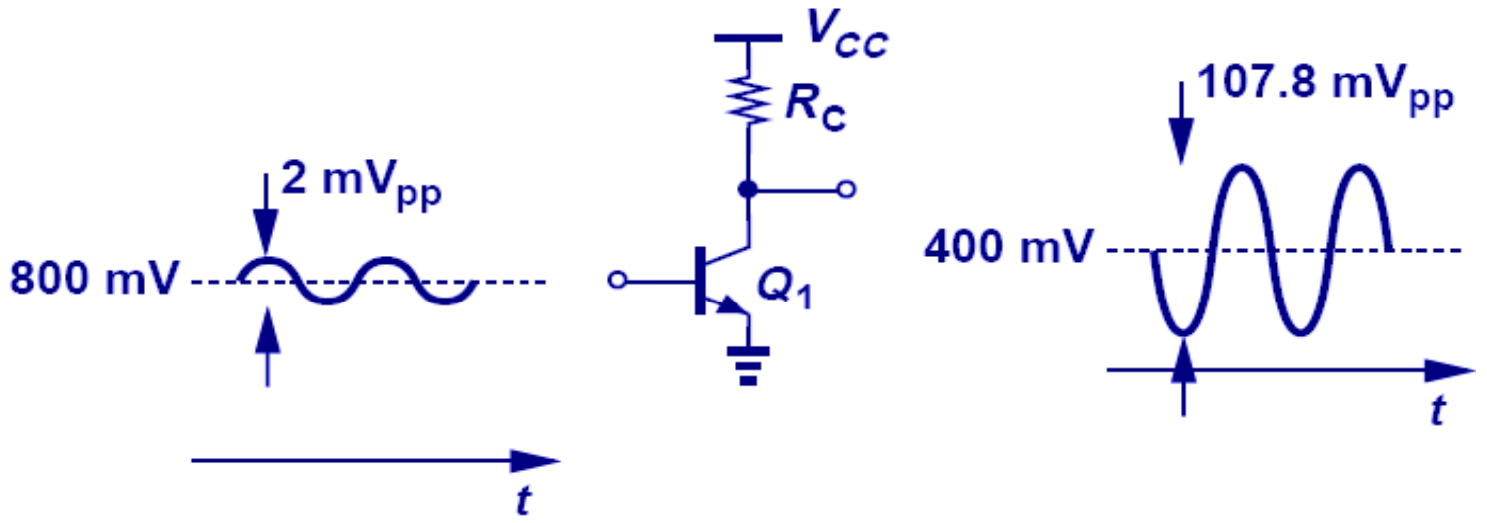
$$A_v = -53.9. \qquad (126)$$

Of course, the circuit can now tolerate only very small voltage swings at the output. For example, a 2-mV_{pp} input signal gives rise to a 107.8-mV_{pp} output, driving Q_1 into heavy saturation [Fig. 5.31(b)]. We say the circuit suffers from a trade-off between voltage gain and voltage "***headroom***."

Tradeoff between Voltage Gain and Headroom



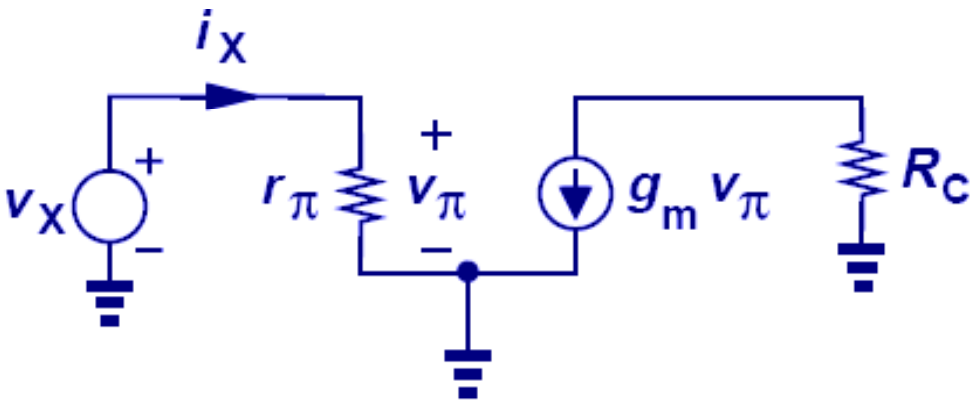
(a)



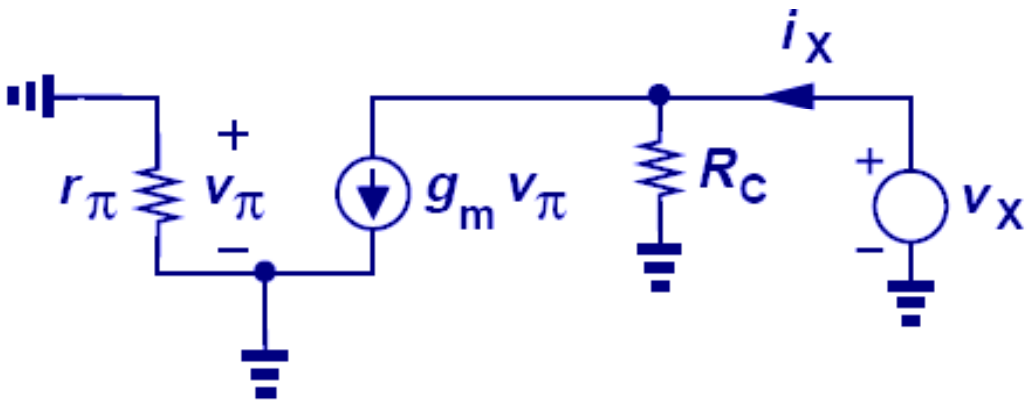
(b)

I/O Impedances of CE Stage

- When measuring output impedance, the input port has to be grounded so that $V_{in} = 0$.



(a)



(b)

$$R_{in} = \frac{v_X}{i_X} = r_\pi = \frac{\beta}{g_m} = \frac{\beta V_T}{I_C}$$

$$R_{out} = \frac{v_X}{i_X} = R_C$$

Example 5.20

A CE stage must achieve an input impedance of R_{in} and an output impedance of R_{out}. What is the voltage gain of the circuit?

Solution

Since $R_{in} = r_\pi = \beta/g_m$ and $R_{out} = R_C$, we have

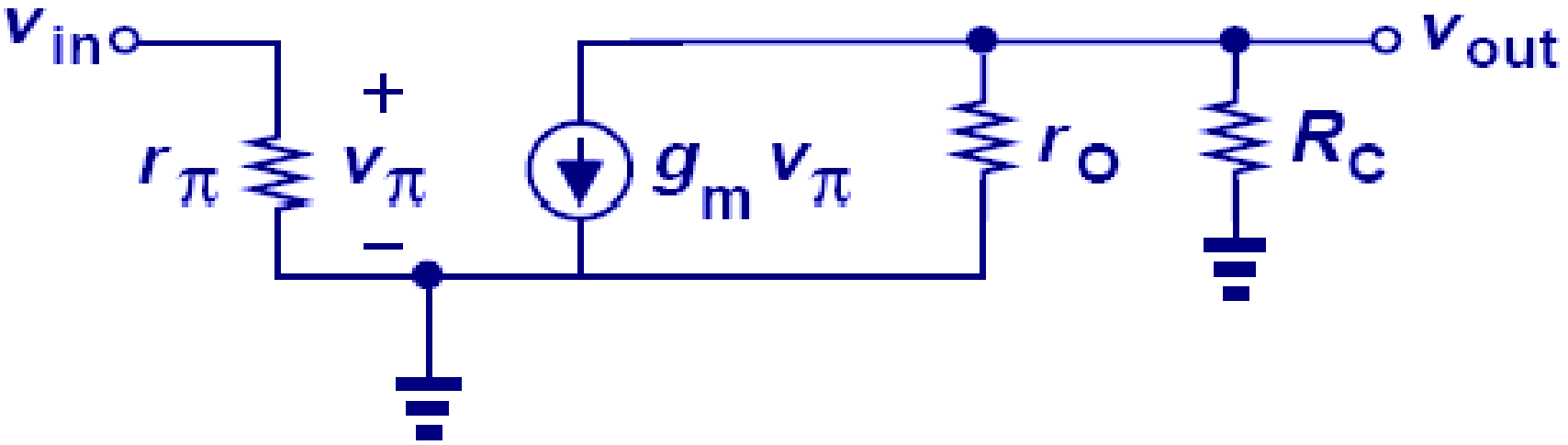
$$A_v = -g_m R_C \tag{131}$$

$$= -\beta \frac{R_{out}}{R_{in}}. \tag{132}$$

Interestingly, if the I/O impedances are specified, then the voltage gain is automatically set. We will develop other circuits in this book that avoid this "coupling" of design specifications.

Inclusion of Early Effect

- Early effect will lower the gain of the CE amplifier, as r_O appears in parallel with R_C.
- The output impedance decreaases.



$$A_v = -g_m(R_C \| r_O)$$

$$R_{out} = R_C \| r_O$$

Example 5.21

The circuit of Fig. 5.29 is biased with a collector current of 1 mA and $R_C = 1$ kΩ. If $\beta = 100$ and $V_A = 10$ V, determine the small-signal voltage gain and the I/O impedances.

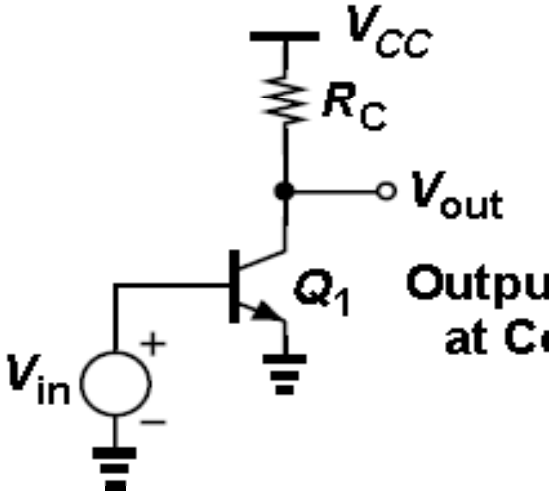
Solution

We have

$$g_m = \frac{I_C}{V_T} = (26\Omega)^{-1}$$

and

$$r_O = \frac{V_A}{I_C} = 10\text{k}\Omega.$$



Thus,

$$A_v = -g_m(R_C \,||\, r_O) \approx 35.$$

(As a comparison, if $V_A = \infty$, then $A_v \approx 38$.) For the I/O impedances, we write

$$R_{in} = r_\pi = \frac{\beta}{g_m} = 2.6\text{k}\Omega$$

and

$$R_{out} = R_C \,||\, r_O = 0.91\text{k}\Omega.$$

Intrinsic Gain

- As R_C goes to infinity, the voltage gain reaches the product of g_m and r_O, which represents the maximum voltage gain the amplifier can have.
- The intrinsic gain is independent of the bias current.
- V_A falls in the vicinity of 5 V, yielding a gain of nearly 200 (actually about 50).
- In this book, we assume $g_m r_O >> 1$ (and hence $r_O >> 1/g_m$) for all transistors.

$$A_v = -g_m r_O \qquad g_m = I_C / V_T$$

$$|A_v| = \frac{V_A}{V_T} \qquad r_O = V_A / I_C$$

Current Gain

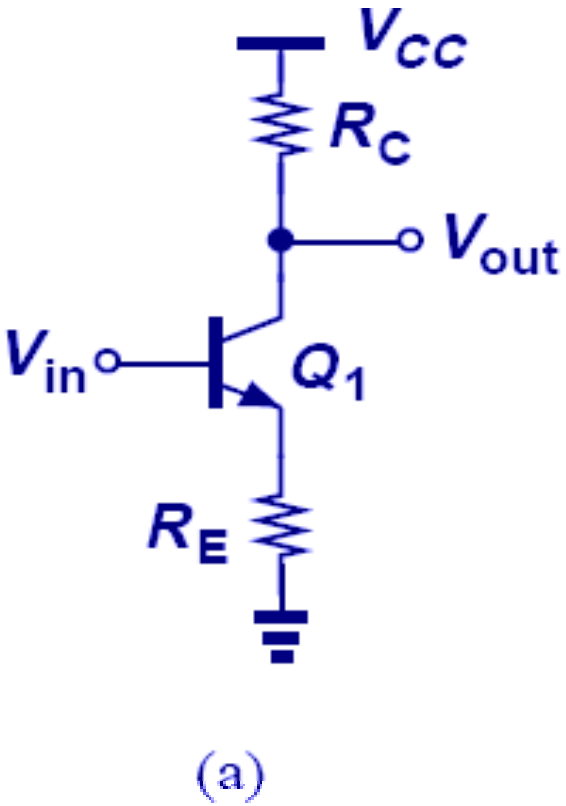
- Another parameter of the amplifier is the current gain, which is defined as the ratio of current delivered to the load to the current flowing into the input.
- For a CE stage, it is equal to β.

$$A_I = \frac{i_{out}}{i_{in}}$$

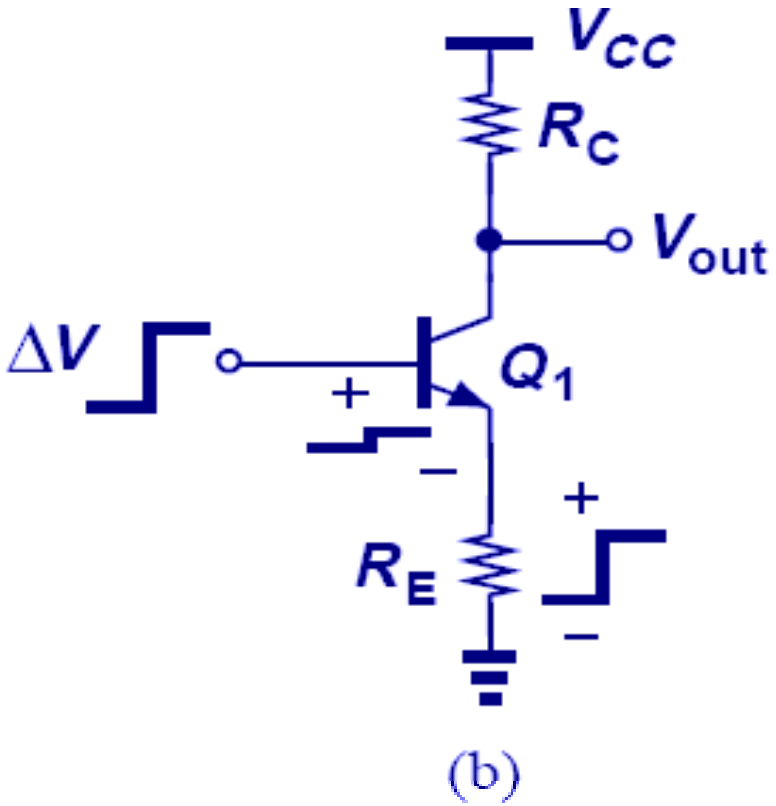
$$A_I\Big|_{CE} = \beta$$

CE with Emitter Degeneration

- By inserting a resistor in series with the emitter, we "*degenerate*" the CE stage.
- This topology will decrease the *gain* of the amplifier but improve other aspects, such as *linearity*, and *input impedance*.



(a)



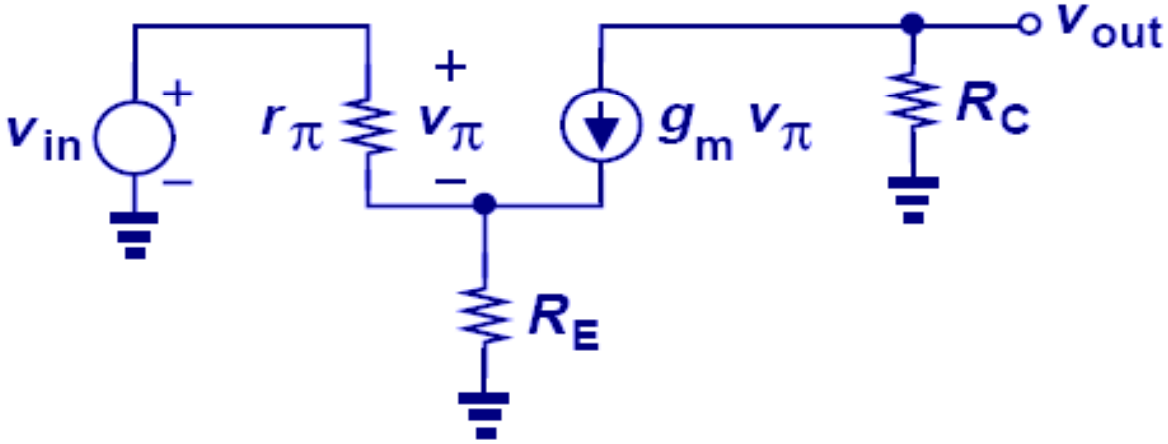
(b)

Small-Signal Model

- the gain falls by a factor of $1 + g_m R_E$
- Interestingly, this gain is equal to the total load resistance to ground divided by $1/g_m$ plus the total resistance placed in series with the emitter.

$$g_m v_\pi = -\frac{v_{out}}{R_C}, \quad v_\pi = -\frac{v_{out}}{g_m R_C}.$$

$$v_{RE} = \left(\frac{v_\pi}{r_\pi} + g_m v_\pi \right) R_E.$$



$$v_{in} = v_\pi + v_{RE} = v_\pi \left[1 + \left(\frac{1}{r_\pi} + g_m \right) R_E \right].$$

$$\frac{v_{out}}{v_{in}} = -\frac{g_m R_C}{1 + \left(\frac{1}{r_\pi} + g_m \right) R_E}.$$

$$A_v = -\frac{g_m R_C}{1 + g_m R_E}$$

$$A_v = -\frac{R_C}{\frac{1}{g_m} + R_E}$$

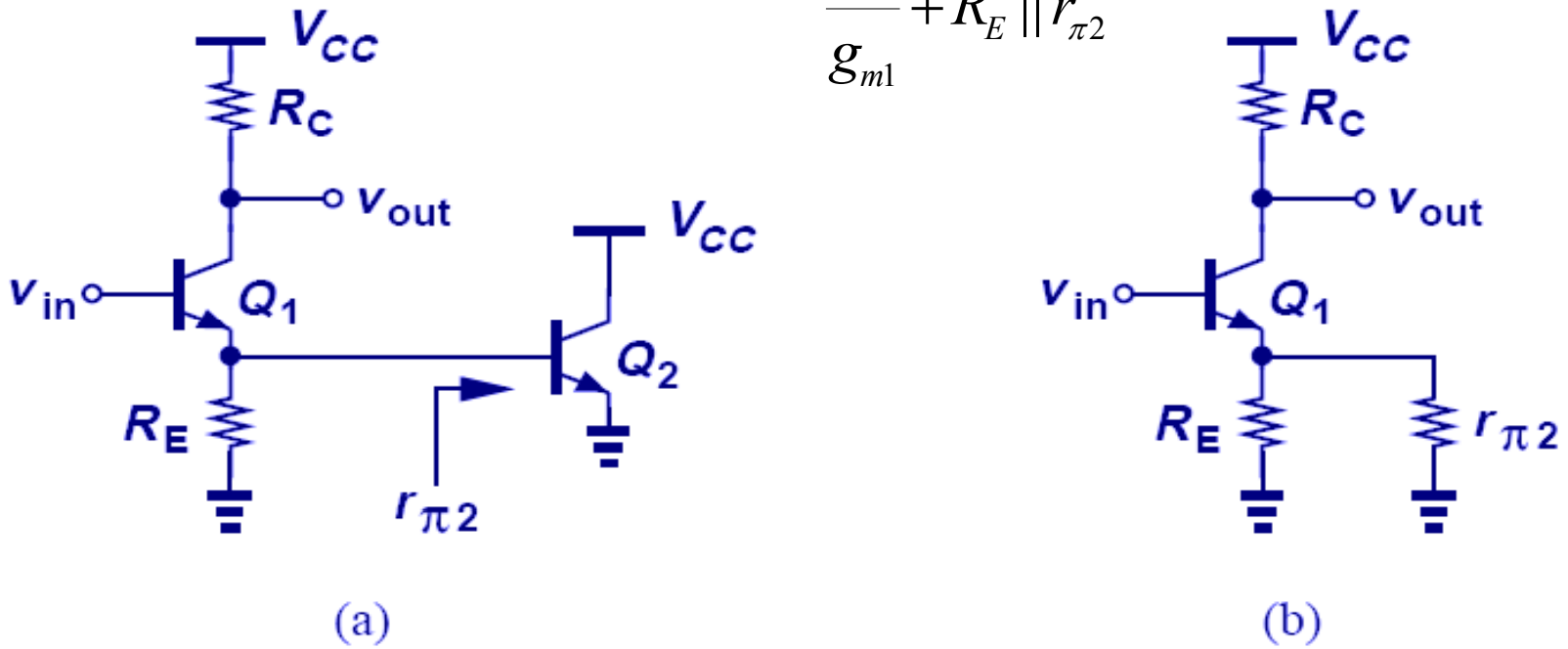
Example 5.22

Determine the voltage gain of the stage shown in Fig. 5.37(a).

Solution

We identify the circuit as a CE stage because the input is applied to the base of Q_1 and the output is sensed at its collector. This transistor is degenerated by two devices: R_E and the base-emitter junction of Q_2. The latter exhibits an impedance of $r_{\pi 2}$, leading to the simplified model depicted in Fig. 5.37(b). The total resistance placed in series with the emitter is therefore equal to $R_E \| r_{\pi 2}$, yielding

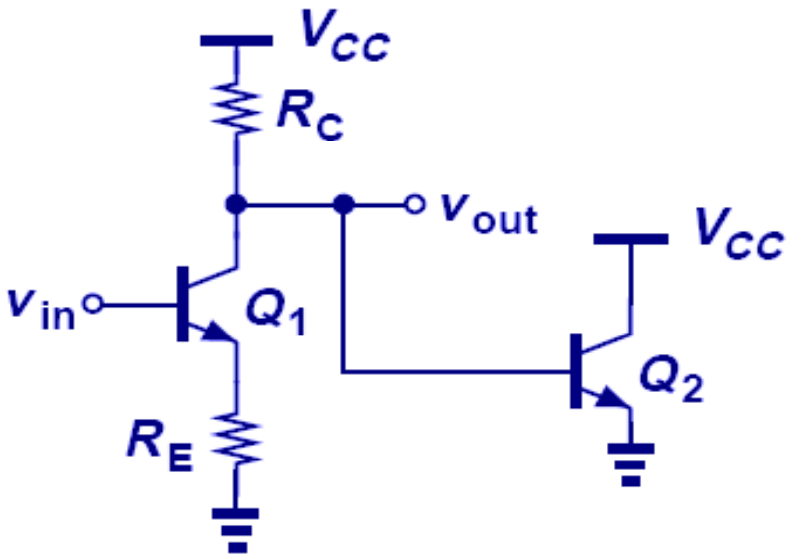
$$A_v = -\frac{R_C}{\frac{1}{g_{m1}} + R_E \| r_{\pi 2}}$$



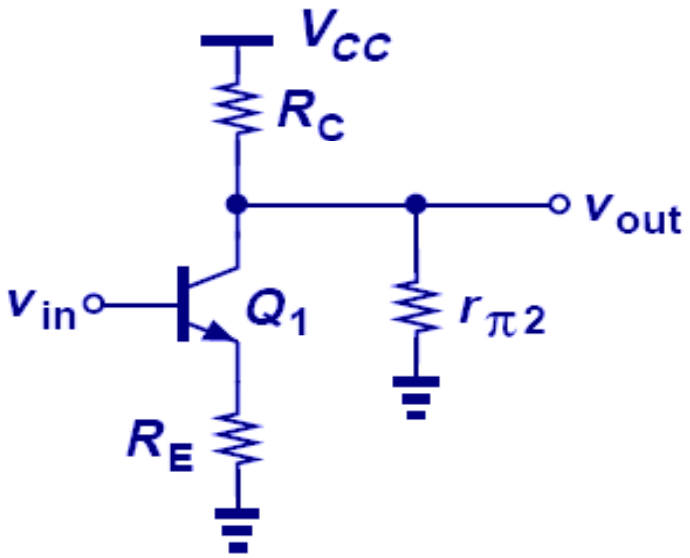
(a) (b)

Emitter Degeneration Example II

- In this example, the input impedance of Q_2 can be combined in parallel with R_C to yield an equivalent collector impedance to ground.



(a)

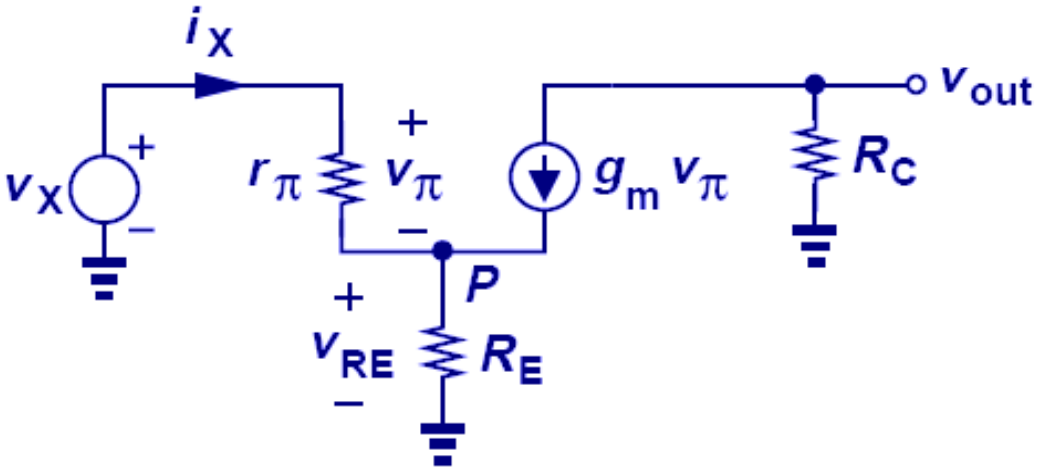


(b)

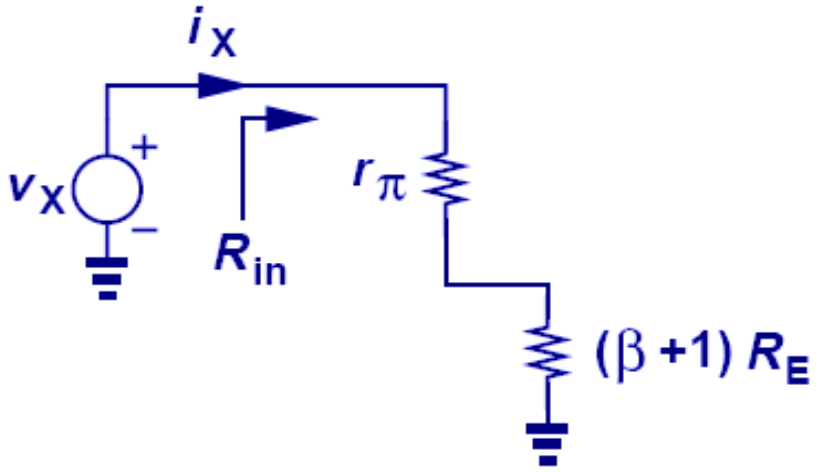
$$A_v = -\frac{R_C \parallel r_{\pi 2}}{\frac{1}{g_{m1}} + R_E}$$

Input Impedance of Degenerated CE Stage

- With emitter degeneration, the input impedance is increased from r_π to $r_\pi + (\beta+1)R_E$; a desirable effect.
- Any impedance tied between the emitter and ground is multiplied by **$(\beta + 1)$** when "seen from the base."



(a)



(b)

$$v_\pi = r_\pi i_X$$

$$i_X + g_m r_\pi i_X = (1+\beta) i_X$$

$$v_{RE} = R_E (1+\beta) i_X$$

$$v_X = v_\pi + v_{RE}$$

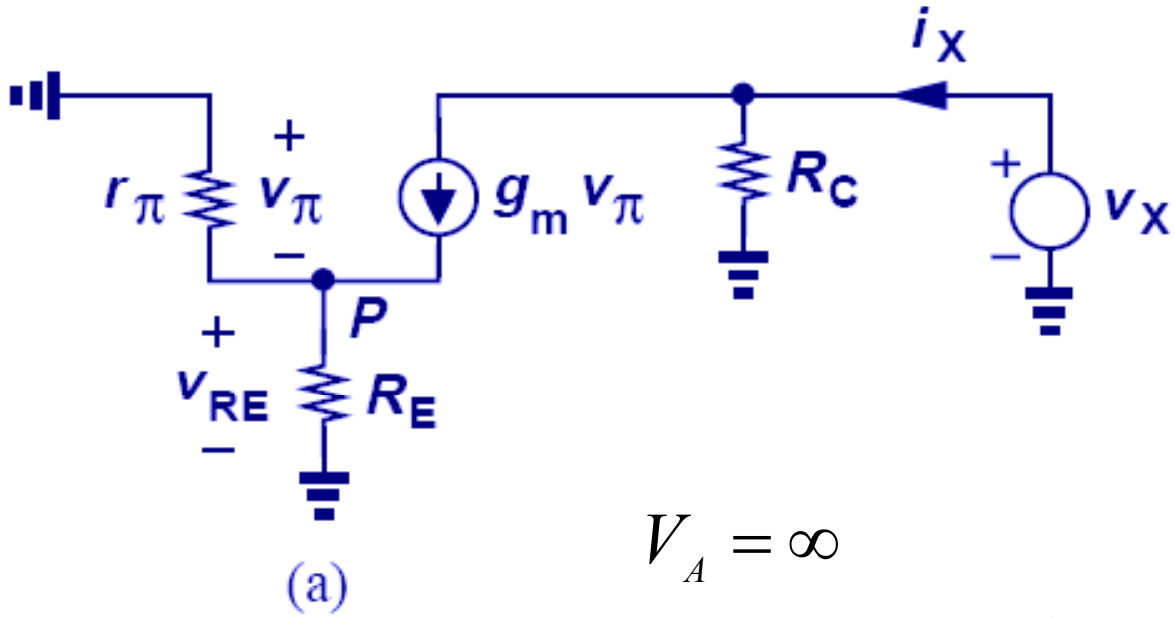
$$V_A = \infty$$

$$v_X = r_\pi i_X + R_E (1+\beta) i_X$$

$$R_{in} = \frac{v_X}{i_X} = r_\pi + (\beta+1) R_E$$

Output Impedance of Degenerated CE Stage

- Emitter degeneration does not alter the output impedance in this case. (More on this later.)



(a)

$$V_A = \infty$$

$$v_{in} = 0 = v_\pi + \left(\frac{v_\pi}{r_\pi} + g_m v_\pi \right) R_E \Rightarrow v_\pi = 0$$

$$R_{out} = \frac{v_X}{i_X} = R_C$$

Example 5.24

A CE stage is biased at a collector current of 1 mA. If the circuit provides a voltage gain of 20 with no emitter degeneration and 10 with degeneration, determine R_C, R_E, and the I/O impedances. Assume $\beta = 100$.

Solution

For $A_v = 20$ in the absence of degeneration, we require $g_m R_C = 20$, which, together with $g_m = I_C/V_T = (26\Omega)^{-1}$, yields $R_C = 520\ \Omega$.

Since degeneration lowers the gain by a factor of two, $1 + g_m R_E = 2$, i.e., $R_E = 1/g_m = 26\Omega$

The input impedance is given by

$$R_{in} = r_\pi + (\beta+1)R_E = \frac{\beta}{g_m} + (\beta+1)R_E \approx 2r_\pi$$

because $\beta >> 1$ and $R_E = 1/g_m$ in this example. Thus, $R_{in} = 5200\ \Omega$. Finally,

$R_{out} = R_C = 520\ \Omega$

Capacitor at Emitter

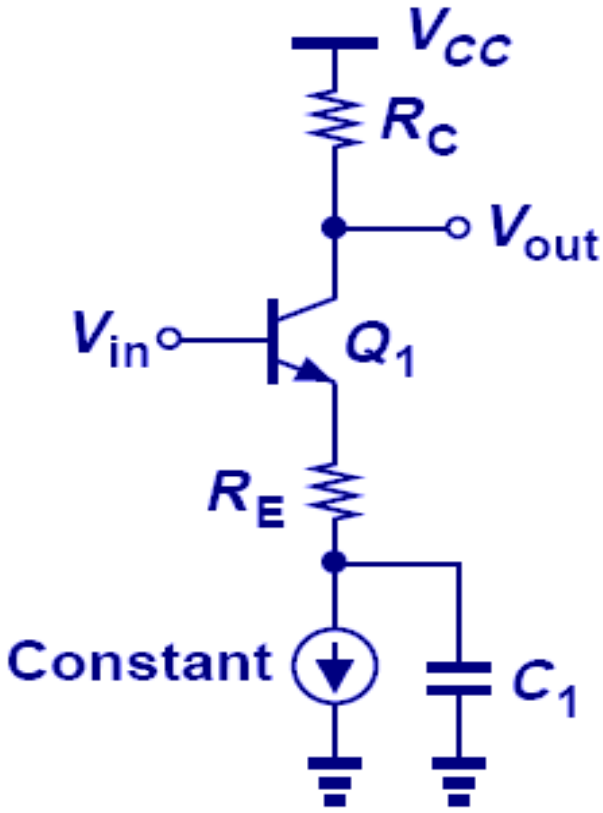
- At DC the capacitor is open and the current source biases the amplifier.
- For ac signals, the capacitor is short and the amplifier is degenerated by R_E.

Example 5.25

Compute the voltage gain and I/O impedances of the circuit depicted in Fig. 5.41. Assume a very large value for C_1.

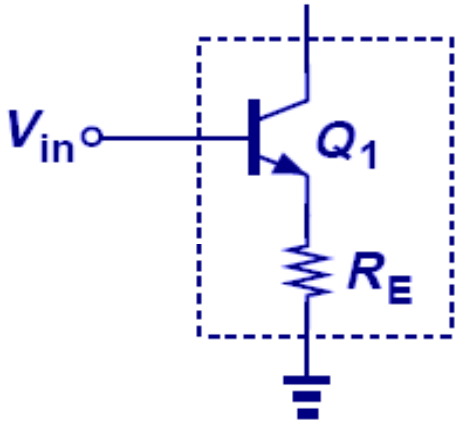
Solution

If C_1 is very large, it acts as a short circuit for the signal frequencies of interest. Also, the constant current source is replaced with an open circuit in the small-signal equivalent circuit. Thus, the stage reduces to that in Fig. 5.35(a) and Eqs. (5.157), (5.162), (5.165) apply.

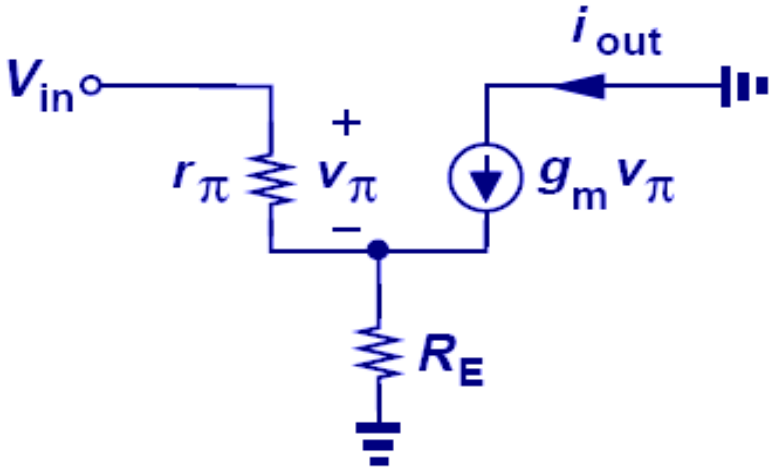


Design CE Stage with Degeneration as a Black Box

- If $g_m R_E$ is much greater than unity, G_m is more linear.



(a)



(b)

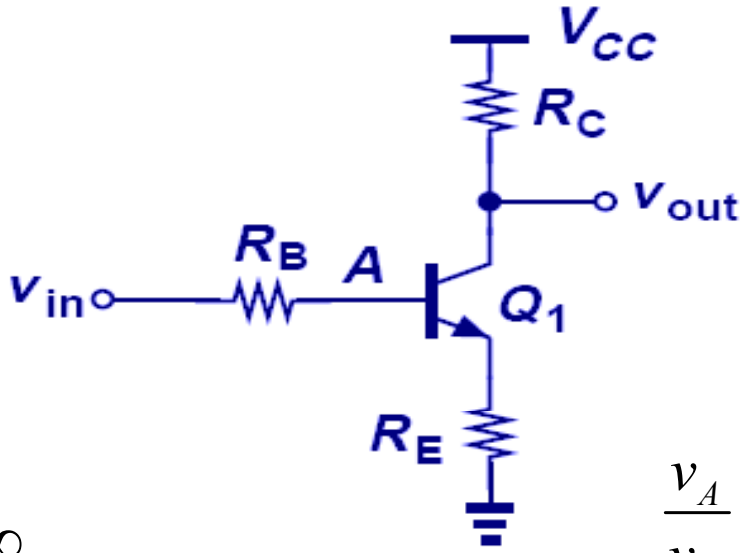
$$V_A = \infty$$

$$i_{out} = g_m \frac{v_{in}}{1 + (r_\pi^{-1} + g_m) R_E}$$

$$G_m = \frac{i_{out}}{v_{in}} \approx \frac{g_m}{1 + g_m R_E}$$

- As $g_m R_E >> 1$, $G_m \approx 1/R_E$
- Then the voltage gain of the stage with a load resistance of R_C is given by $A_v \approx - R_C/R_E$

Degenerated CE Stage with Base Resistance

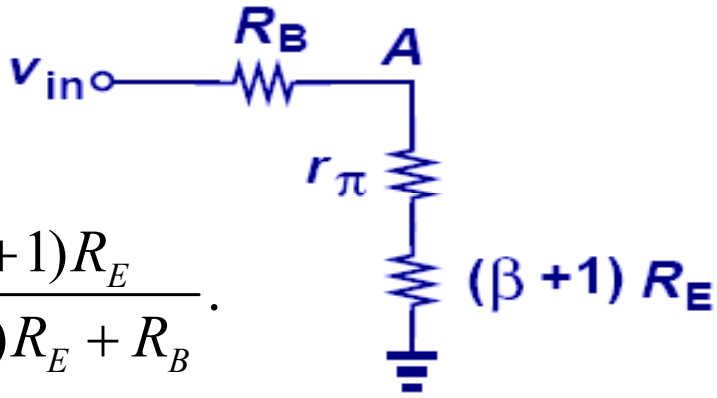


$$V_A = \infty$$

$$\frac{v_{out}}{v_{in}} = \frac{v_A}{v_{in}} \cdot \frac{v_{out}}{v_A}$$

$$\frac{v_{out}}{v_{in}} = \frac{-\beta R_C}{r_\pi + (\beta+1)R_E + R_B}$$

$$A_v \approx \frac{-R_C}{\frac{1}{g_m} + R_E + \frac{R_B}{\beta+1}}$$



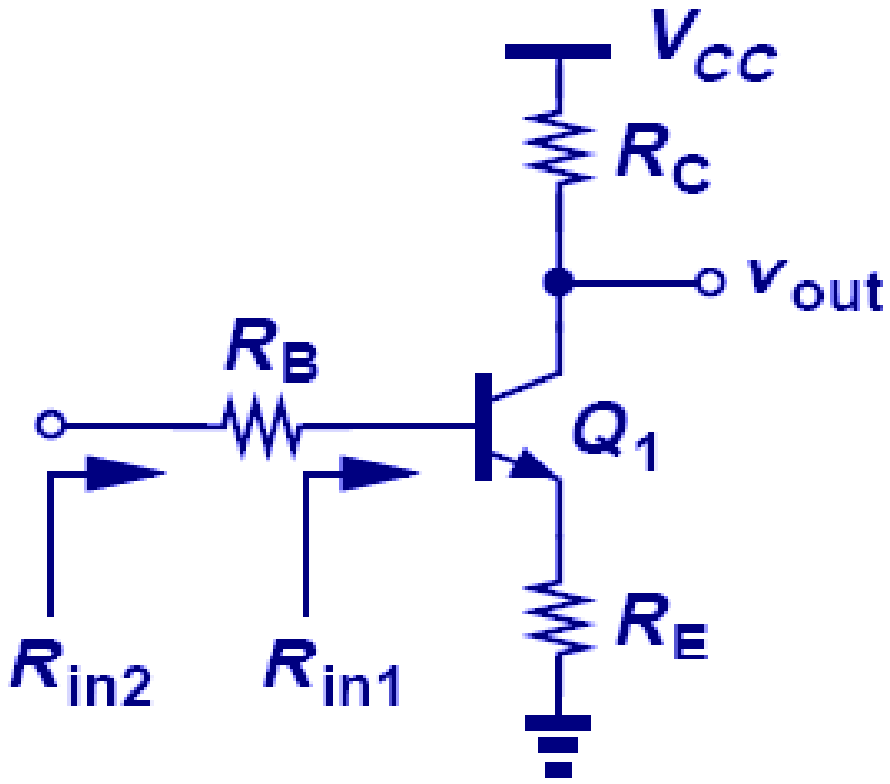
$$\frac{v_A}{v_{in}} = \frac{r_\pi + (\beta+1)R_E}{r_\pi + (\beta+1)R_E + R_B}.$$

$$\frac{v_{out}}{v_{in}} = \frac{r_\pi + (\beta+1)R_E}{r_\pi + (\beta+1)R_E + R_B} \cdot \frac{-g_m R_C}{1 + \left(\frac{1}{r_\pi} + g_m\right) R_E}$$

- R_B only *degrades* the performance of the circuit, but often proves inevitable.
- For example, R_B may represent the output resistance of a microphone connected to the input of the amplifier.
- R_B is scaled down by $\beta + 1$

Input/Output Impedances

- R_{in1} is more important in practice as R_B is often the output impedance of the previous stage.



$$V_A = \infty$$

$$R_{in1} = r_\pi + (\beta + 1)R_E$$

$$R_{in2} = R_B + r_{\pi 2} + (\beta + 1)R_E$$

$$R_{out} = R_C$$

Example 5.26

A microphone having an output resistance of 1 kΩ generates a peak signal level of 2 mV. Design a CE stage with a bias current of 1 mA that amplifies this signal to 40 mV. Assume $R_E = 4/g_m$ and $\beta = 100$.

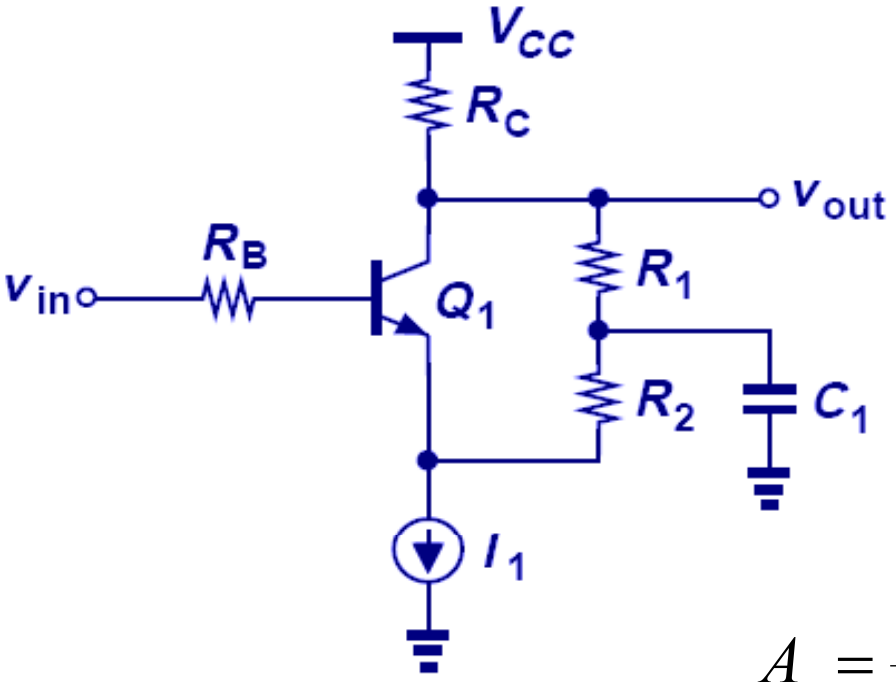
Solution

The following quantities are obtained: $R_B = 1$ kΩ, $g_m = (26\Omega)^{-1}$, $|A_v| = 20$, and $R_E = 104\Omega$. From Eq. (5.185),

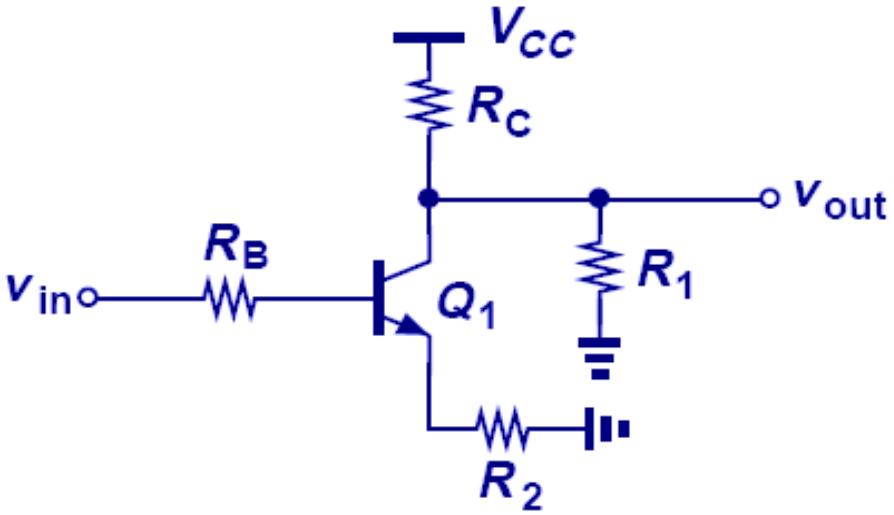
$$R_C = |A_v| \left(\frac{1}{g_m} + R_E + \frac{R_B}{\beta + 1} \right) \approx 2.8\text{k}\Omega.$$

Example 5.27

- Assume a very large value for C_1 and neglect the Early effect.
- Replacing C_1 with a short circuit, I_1 with an open circuit, and V_{CC} with ac ground, we arrive at the simplified model in Fig. (b).



(a)



(b)

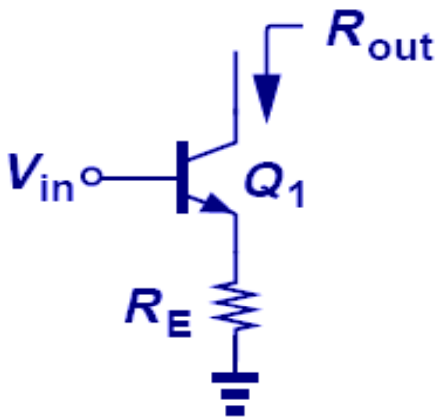
$$A_v = \frac{-(R_C \parallel R_1)}{\frac{1}{g_m} + R_2 + \frac{R_B}{\beta+1}}$$

$$R_{in} = r_\pi + (\beta+1)R_2$$

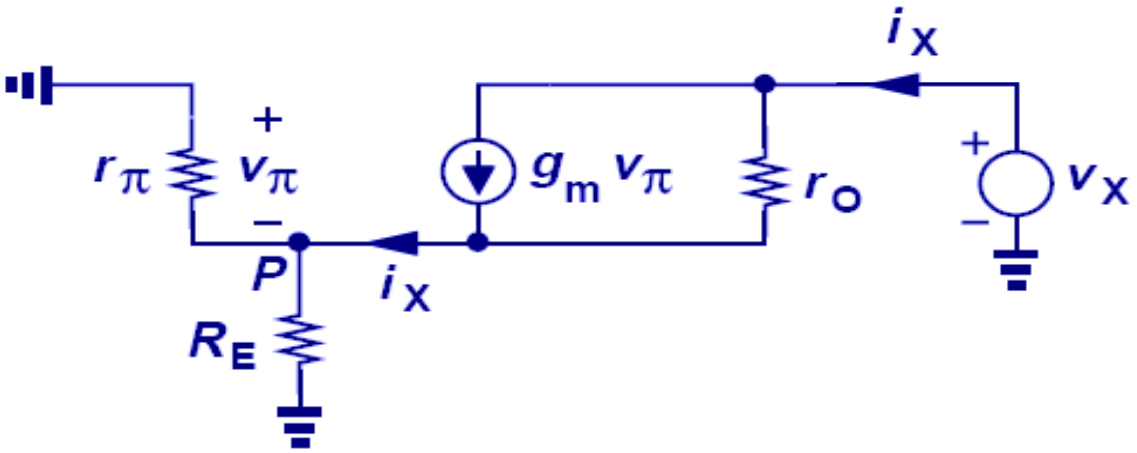
$$R_{out} = R_C \parallel R_1$$

Early Effect on Output Impedance ($V_A < \infty$)

- Emitter degeneration *boosts* the output impedance by a factor of $1+g_m(R_E||r_\pi)$.
- This improves the gain of the amplifier and makes the circuit a better current source.



(a)



(b)

R_{out} looking into the collector of a degenerated transistor, R_E :

$R_{out} = r_O$, if $R_E = 0$.

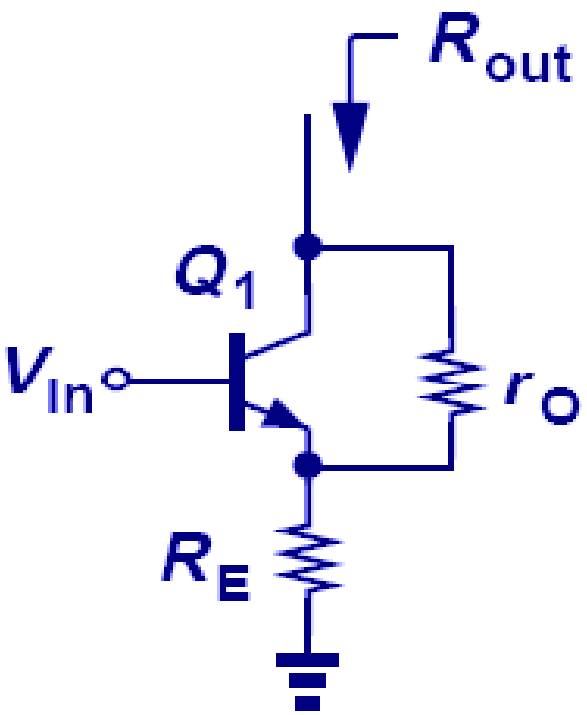
$R_{out} = \infty$, if $V_A = \infty$.

$$R_{out} = [1 + g_m(R_E \| r_\pi)]r_O + R_E \| r_\pi$$

$$R_{out} = r_O + (g_m r_O + 1)(R_E \| r_\pi)$$

$$R_{out} \approx r_O[1 + g_m(R_E \| r_\pi)]$$

Two Special Cases



$$R_{out} = [1 + g_m(R_E \| r_\pi)]r_O + R_E \| r_\pi$$

1) $R_E >> r_\pi$

$$R_{out} \approx r_O(1 + g_m r_\pi) \approx \beta r_O$$

2) $R_E << r_\pi$

$$R_{out} \approx (1 + g_m R_E)r_O$$

1) the maximum resistance seen at the collector is βr_O

2) the output resistance is boosted by a factor of $1+g_m R_E$

Example 5.28

We wish to design a current source having a value of 1 mA and an output resistance of 20 kΩ. The available bipolar transistor exhibits $\beta = 100$ and $V_A = 10$V. Determine the minimum required value of emitter degeneration resistance.

Solution

Since $r_O = V_A/I_C = 10$ kΩ, degeneration must raise the output resistance by a factor of two. We postulate that the condition $R_E << r_\pi$ holds and write

$$1 + g_m R_E = 2$$

That is,

$$R_E = 1/g_m = 26\ \Omega$$

Note that indeed $r_\pi = \beta/g_m >> R_E$.

Example 5.29

Calculate the output resistance of the circuit shown in Fig. 5.48(a) if C_1 is very large.

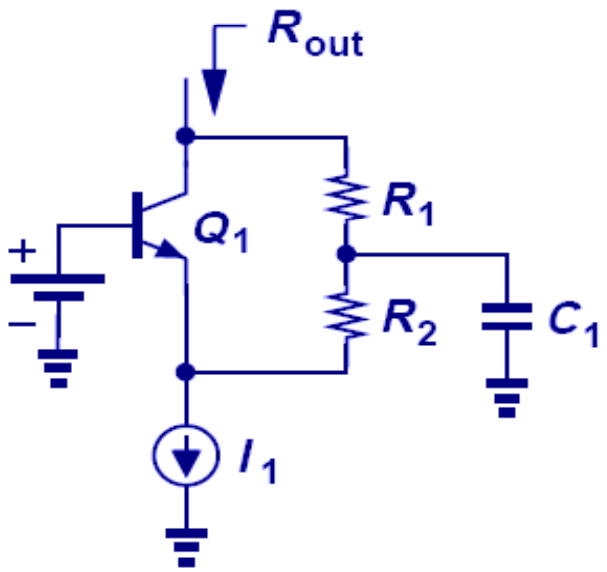
Solution

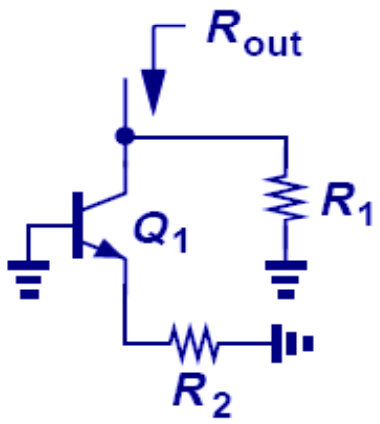
Replacing V_b and C_1 with an ac ground and I_1 with an open circuit, we arrive at the simplified model in Fig. 5.48(b). Since R_1 appears in parallel with the resistance seen looking into the collector of Q_1, we ignore R_1 for the moment, reducing the circuit to that in Fig. 5.48(c). In analogy with Fig. 5.40, we rewrite Eq. (5.200) as

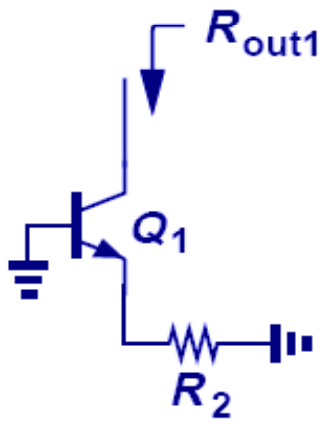
$$R_{out1} = [1 + g_m(R_2 \,||\, r_\pi)]r_O.$$

Returning to Fig. 5.48(b), we have

$$R_{out} = R_{out1} \,||\, R_1 \quad = \{[1 + g_m(R_2 \,||\, r_\pi)]r_O\} \,||\, R_1.$$







Example 5.30

Determine the output resistance of the stage shown in Fig. 5.49(a).

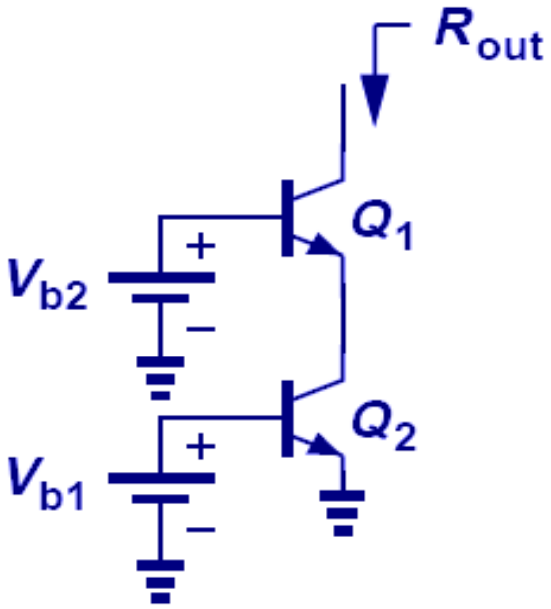
Solution

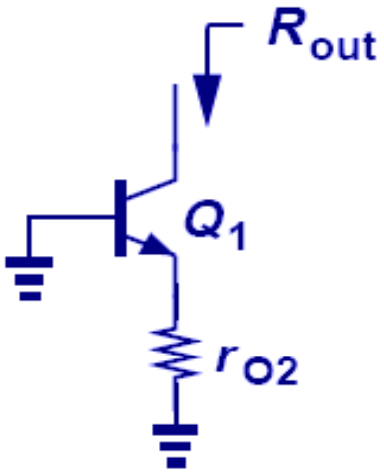
Recall from Fig. 5.7 that the impedance seen at the collector is equal to r_O if the base and emitter are (ac) grounded. Thus, Q_2 can be replaced with r_{O2} [Fig. 5.49(b)]. From another perspective, Q_2 is reduced to r_{O2} because its base-emitter voltage is fixed by V_{b1}, yielding a zero $g_{m2}v_{\pi 2}$.

Now, r_{O2} plays the role of emitter degeneration resistance for Q_2. In analogy with Fig. 5.40(a), we rewrite Eq. (5.200) as

$$R_{out} = [1 + g_{m1}(r_{O2} \| r_{\pi 1})]r_{O1}.$$

Called a "***cascode***" circuit, this topology is studied and utilized extensively in Chapter 9.





Example 5.31

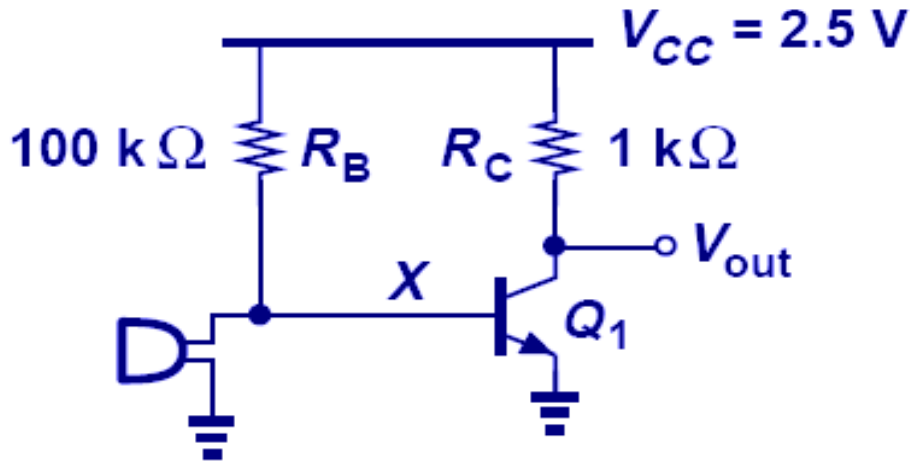
A student familiar with the CE stage and basic biasing constructs the circuit shown in Fig. 5.50 to amplify the signal produced by a microphone. Unfortunately, Q_1 carries no current, failing to amplify. Explain the cause of this problem.

Solution

Many microphones exhibit a small low-frequency resistance (e.g., < 100 Ω). If used in this circuit, such a microphone creates a low resistance from the base of Q_1 to ground, forming a voltage divider with R_B and providing a very low base voltage. For example, a microphone resistance of 100 Ω yields

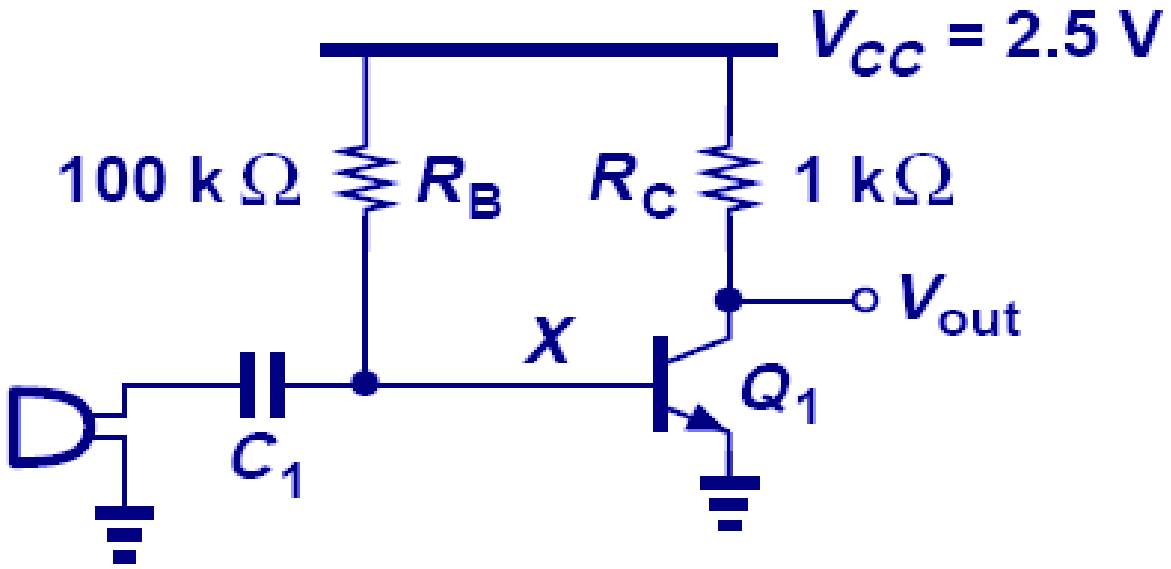
$$V_X = \frac{100\Omega}{100\text{k}\Omega + 100\Omega} \times 2.5\text{V} \approx 2.5\text{mV}.$$

Thus, the microphone low-frequency resistance disrupts the bias of the amplifier.



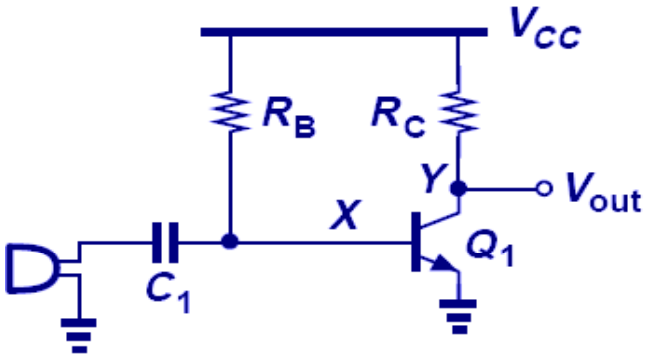
Use of Coupling Capacitor

- Capacitor isolates the bias network from the microphone at DC but shorts the microphone to the amplifier at higher frequencies.
- C_1 is a "***coupling***" capacitor and the input of this stage is "***ac-coupled***" or "*capacitively-coupled*."

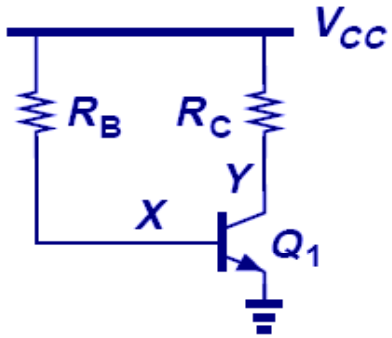


DC and AC Analysis

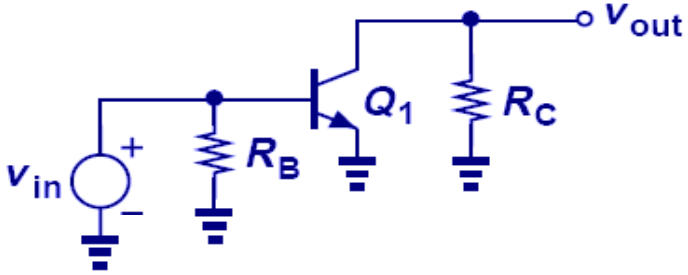
- Coupling capacitor is open for DC calculations and shorted for AC calculations.



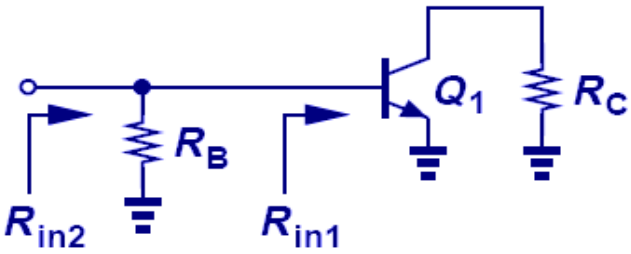
(a)



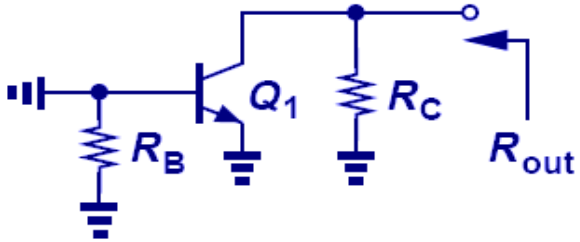
(b) bias calculation



(c) small-signal calculation



(d)



(e)

$$I_C = \beta \frac{V_{CC} - V_{BE}}{R_B},$$

$$V_Y = V_{CC} - \beta R_C \frac{V_{CC} - V_{BE}}{R_B}. \quad V_Y \geq V_{BE}$$

$$A_v = -g_m (R_C \,||\, r_O)$$

$$R_{in} = r_\pi \,||\, R_B$$

$$R_{out} = R_C \,||\, r_O$$

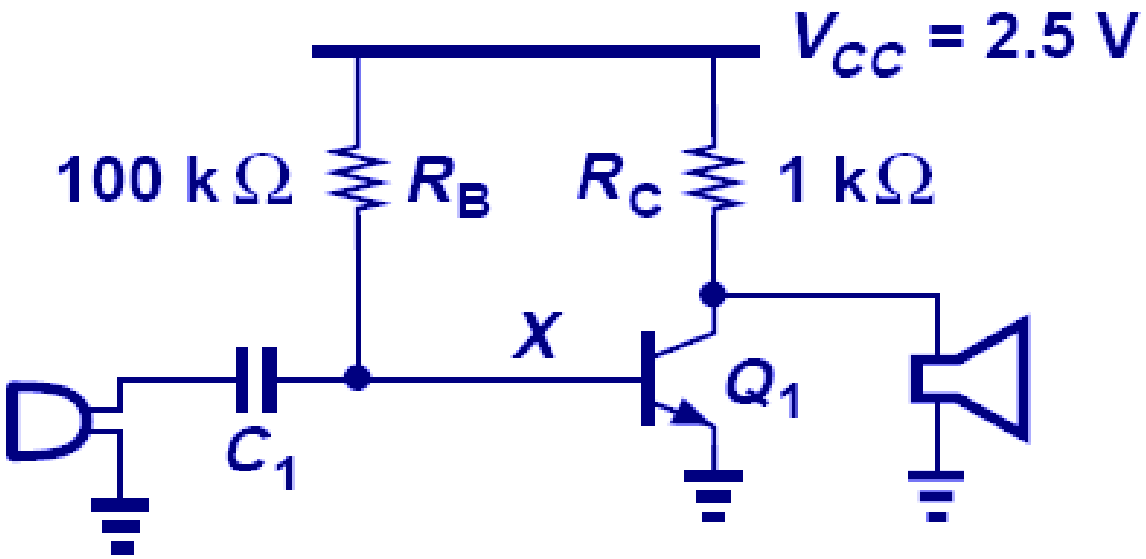
Example 5.32 Bad Output Connection

Having learned about ac coupling, the student in Example 5.31 modifies the design to that shown in Fig. 5.53 and attempts to drive a speaker. Unfortunately, the circuit still fails. Explain why.

Solution

Typical speakers incorporate a solenoid (inductor) to actuate a membrane. The solenoid exhibits a very low dc resistance, e.g., less than 1 Ω. Thus, the speaker in Fig. 5.53 shorts the collector to ground, driving Q_1 into deep saturation.

Since the speaker has an inductor, connecting it directly to the amplifier would short the collector at DC and therefore push the transistor into deep saturation.



Example 5.33 Still No Gain!!!

The student applies ac coupling to the output as well [Fig. 5.54(a)] and measures the quiescent points to ensure proper biasing. The collector bias voltage is 1.5 V, indicating that Q_1 operates in the active region. However, the student still observes no gain in the circuit. (a) If $I_S = 5 \times 10^{-17}$ A and $V_A = \infty$, compute the β of the transistor. (b) Explain why the circuit provides no gain.

Solution

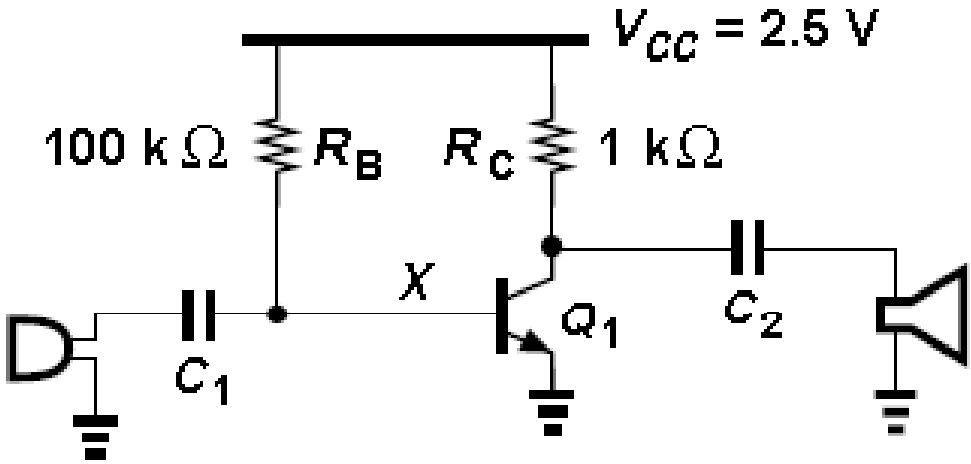
(a) A collector voltage of 1.5 V translates to a voltage drop of 1 V across R_C and hence a collector current of 1 mA. Thus,

$$V_{BE} = V_T \ln \frac{I_C}{I_S} = 796\text{mV}.$$

It follows that

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = 17\,\mu\text{A},$$

and $\beta = I_C / I_B = 58.8$.



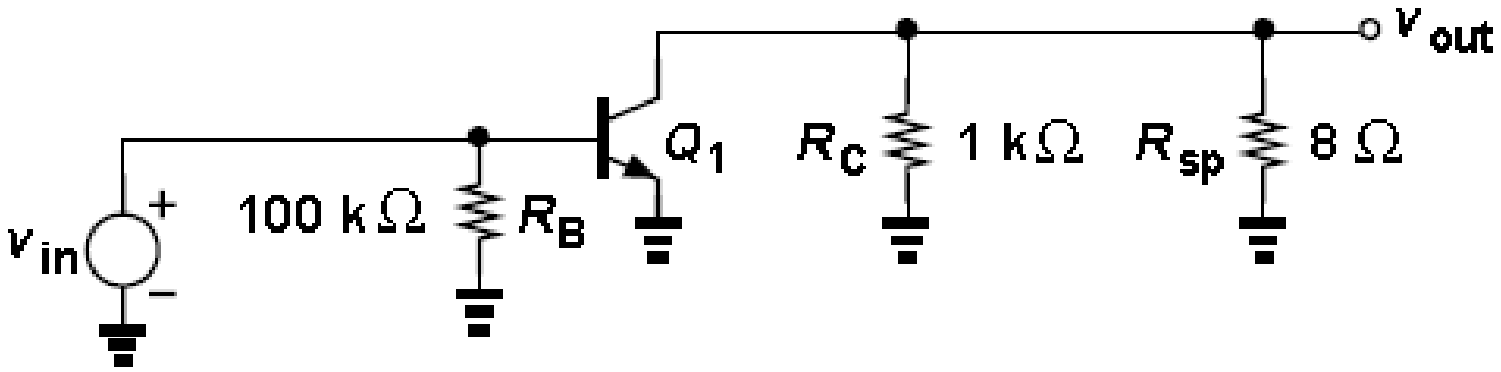
(a)

Example 5.33 (cnt'd)

(b) Speakers typically exhibit a low impedance in the audio frequency range, e.g., 8 Ω. Drawing the ac equivalent as in Fig. 5.54(b), we note that the total resistance seen at the collector node is equal to 1k Ω || 8 Ω, yielding a gain of

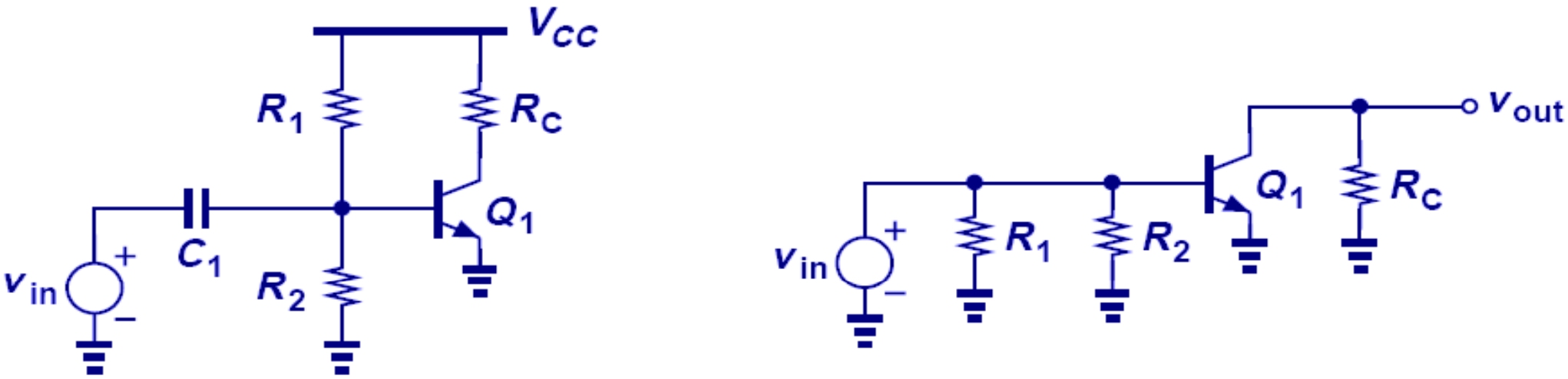
$$|A_v| = g_m(R_C \parallel R_S) = 0.31$$

In this example, the AC coupling indeed allows correct biasing. However, due to the speaker's small input impedance, the overall gain drops considerably.



(b)

CE Stage with Biasing



(a) Biased stage with capacitive coupling, (b) simplified circuit.

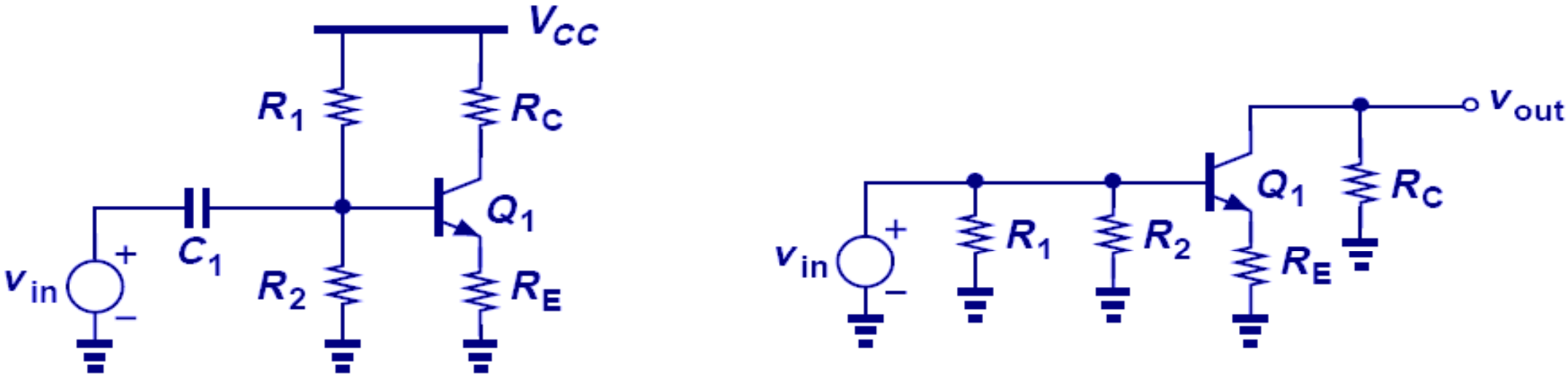
jump to DC bias @ 5-21

$$A_v = -g_m(R_C \parallel r_O)$$

$$R_{in} = r_\pi \parallel R_1 \parallel R_2$$

$$R_{out} = R_C \parallel r_O$$

CE Stage with Robust Biasing



(a) Degenerated stage with capacitive coupling, (b) simplified circuit.

$$A_v = \frac{-R_C}{\frac{1}{g_m} + R_E} \qquad \text{if } V_A = \infty$$

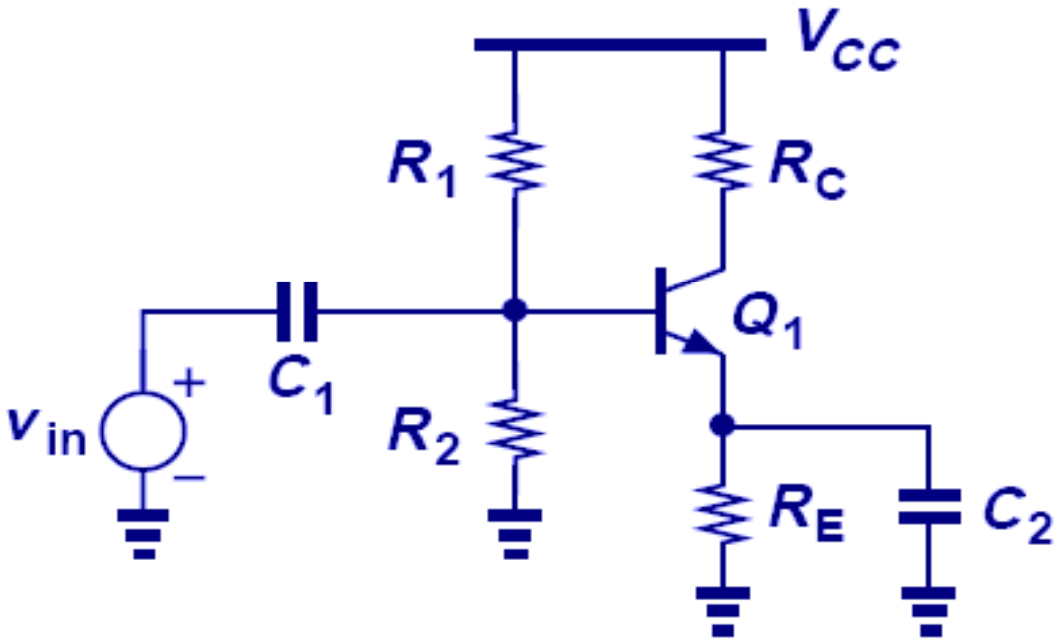
$$R_{in} = [r_\pi + (\beta+1)R_E] \| R_1 \| R_2$$

$$R_{out} = R_C$$

- Emitter degeneration can effectively stabilize the bias point despite variations in β and I_S, but also lower the gain.

Removal of Degeneration for Signals at AC

- Capacitor C_2 shorts out R_E at higher frequencies and removes degeneration at AC, where C_2 is large enough to act as a short circuit for signal frequencies of interest.

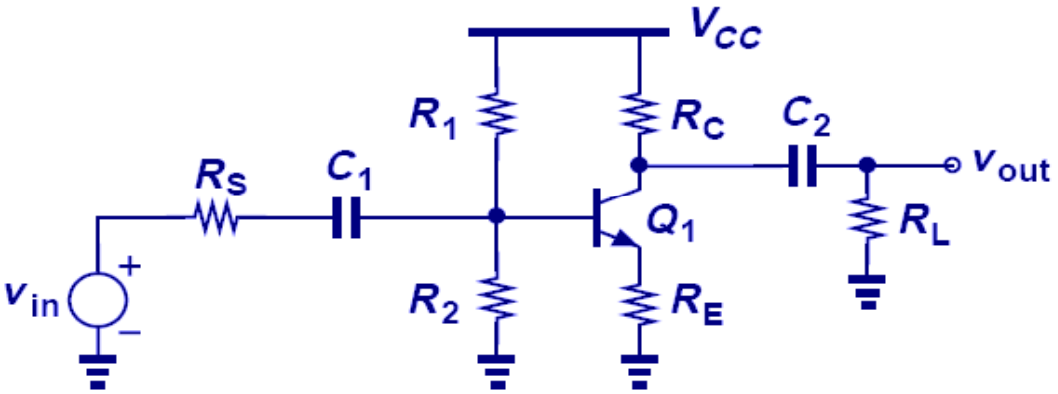


$$A_v = -g_m R_C$$

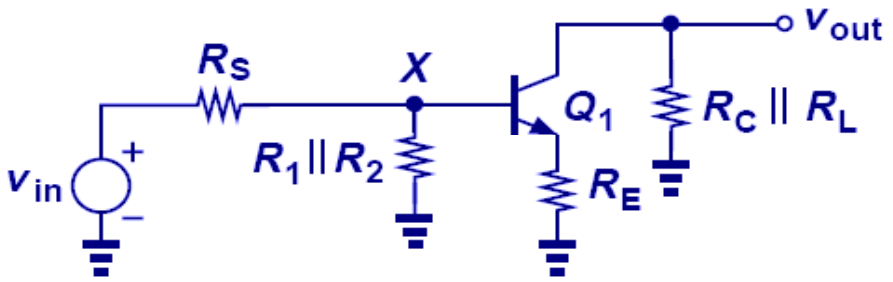
$$R_{in} = r_\pi \parallel R_1 \parallel R_2$$

$$R_{out} = R_C$$

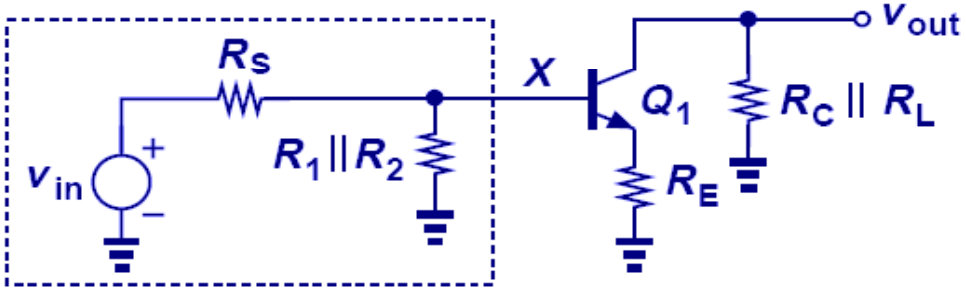
Complete CE Stage



(a)



(b)



(b)

$$v_{Thev} = \frac{R_1 \| R_2}{R_1 \| R_2 + R_S} v_{in}$$

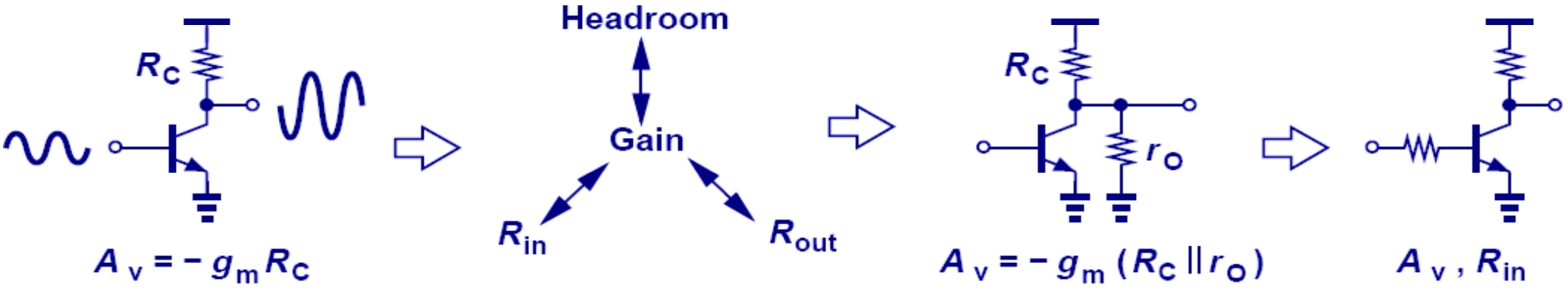
$$R_{Thev} = R_S \| R_1 \| R_2 .$$

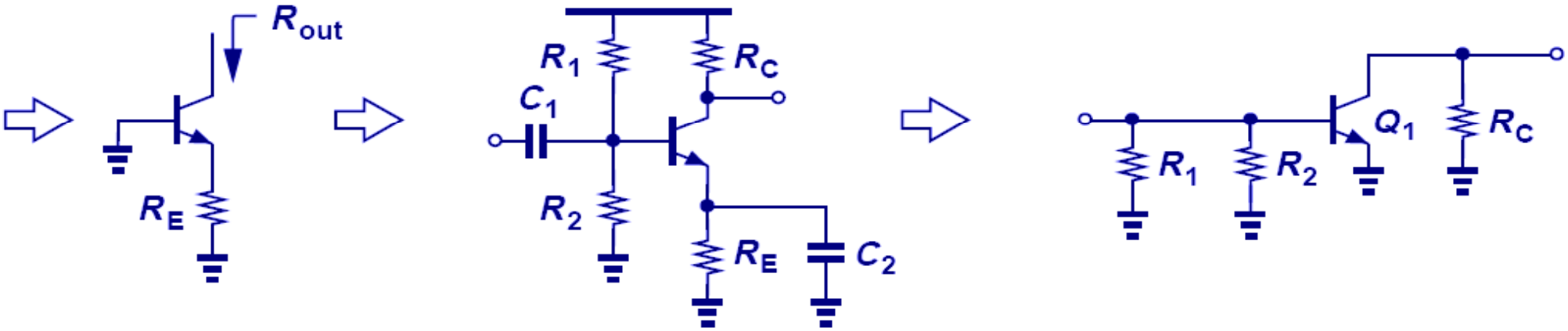
$$\frac{v_X}{v_{in}} = \frac{R_1 \| R_2 \| [r_\pi + (\beta+1)R_E]}{R_1 \| R_2 \| [r_\pi + (\beta+1)R_E] + R_S}.$$

$$A_v = -\frac{R_C \| R_L}{\dfrac{1}{g_m} + R_E + \dfrac{R_{Thev}}{\beta+1}} \cdot \frac{R_1 \| R_2}{R_1 \| R_2 + R_S},$$

$$\frac{v_{out}}{v_{in}} = \frac{v_X}{v_{in}} \cdot \frac{v_{out}}{v_X} = -\frac{R_1 \| R_2 \| [r_\pi + (\beta+1)R_E]}{R_1 \| R_2 \| [r_\pi + (\beta+1)R_E] + R_S} \frac{R_C \| R_L}{\dfrac{1}{g_m} + R_E}.$$

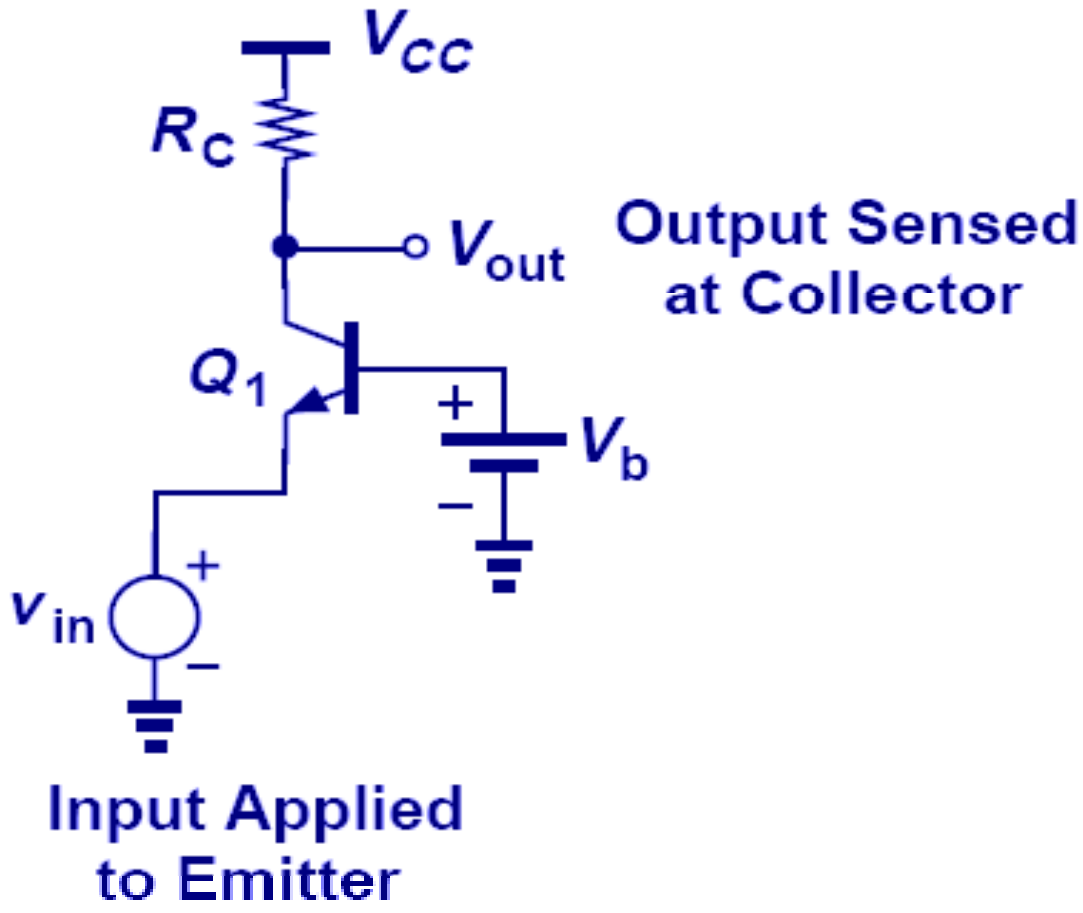
Summary of CE Concepts





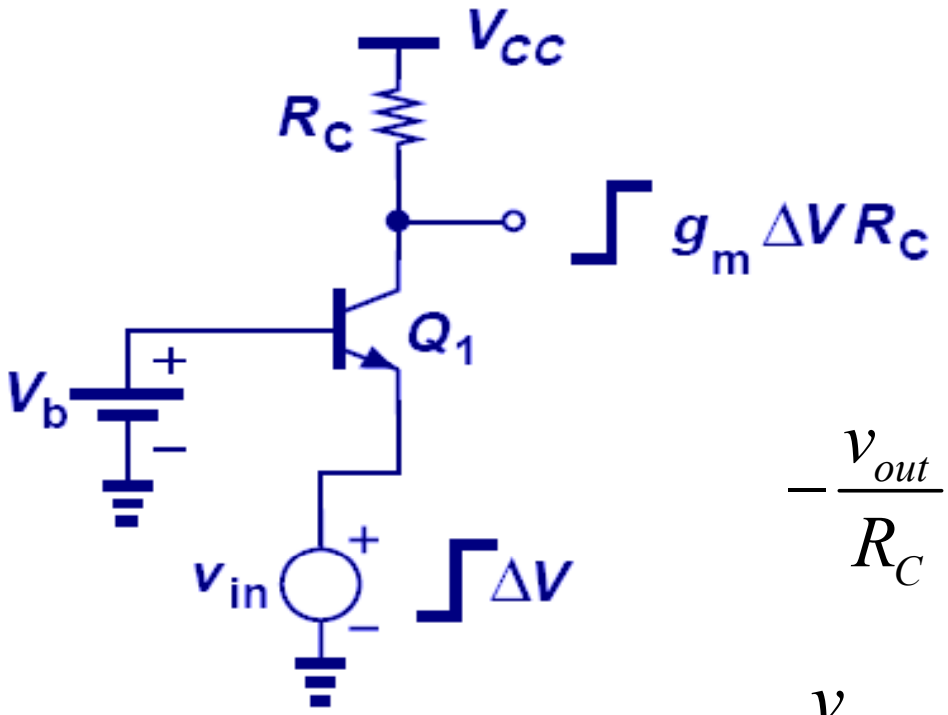
Common Base (CB) Amplifier

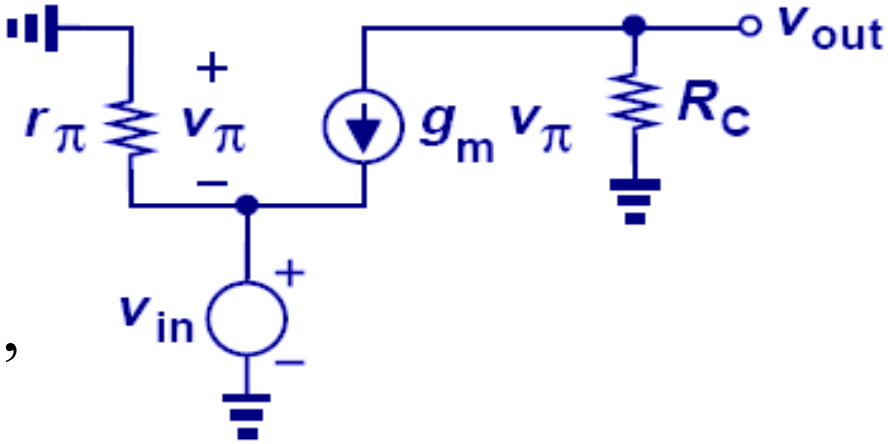
- In common base topology, where the base terminal is biased with a fixed voltage, emitter is fed with an input signal, and collector is the output.



CB Core

- If v_{in} goes up by a small amount ΔV, the base-emitter voltage of Q_1 *decreases* by the same amount because the base voltage is fixed. Consequently, the collector current falls by $g_m \Delta V$, allowing v_{out} to *rise* by $g_m \Delta V R_C$.
- The voltage gain of CB stage is $g_m R_C$, which is identical to that of CE stage in magnitude and opposite in phase.



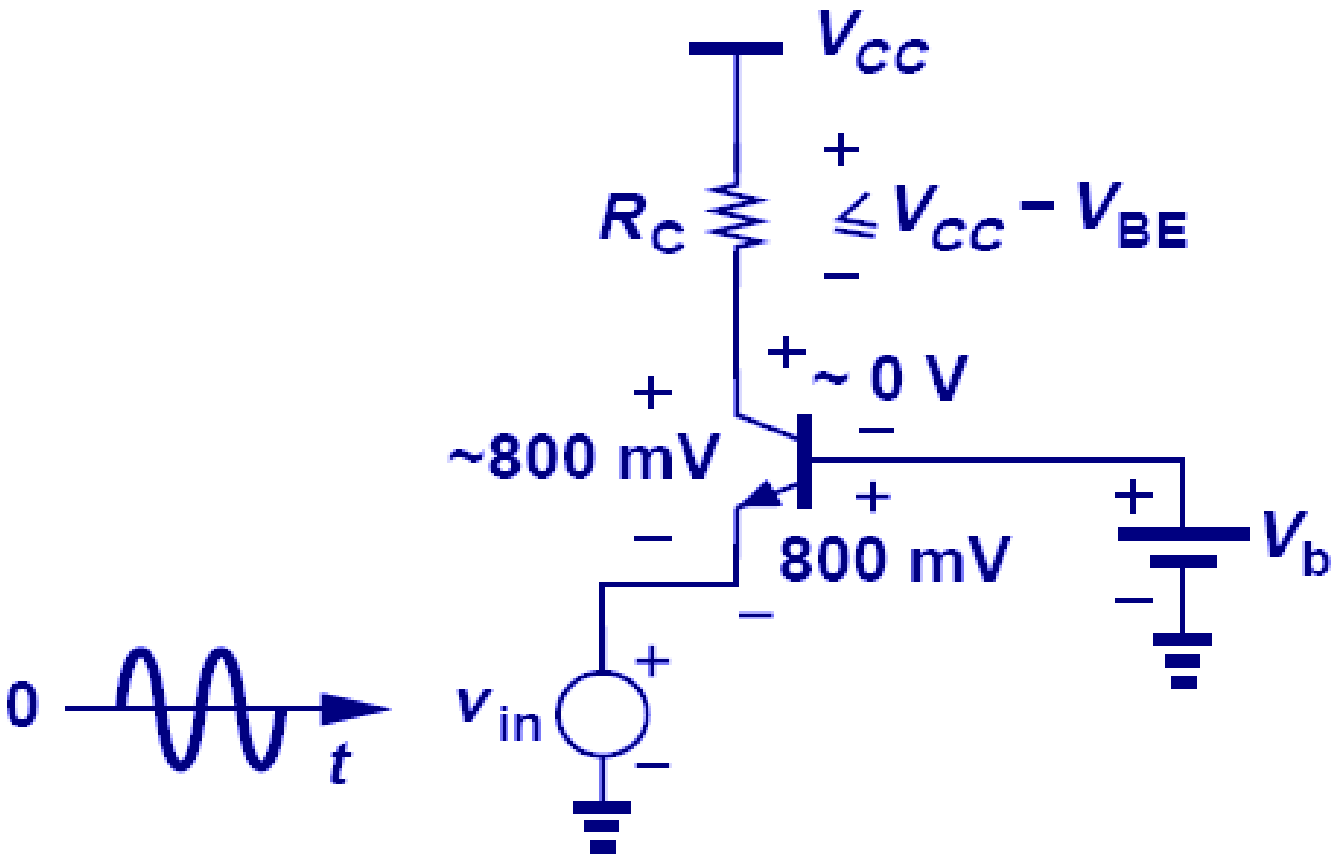


$$-\frac{v_{out}}{R_C} = g_m v_\pi,$$

$$\frac{v_{out}}{v_{in}} = g_m R_C.$$

Tradeoff between Gain and Headroom

- To maintain the transistor out of saturation, the maximum voltage drop across R_C cannot exceed V_{CC}-V_{BE}.



$$A_v = g_m R_C = \frac{I_C}{V_T}.R_C$$

$$= \frac{V_{CC} - V_{BE}}{V_T}$$

Example 5.35

The voltage produced by an electronic thermometer is equal to 600 mV at room temperature. Design a CB stage to sense the thermometer voltage and amplify the change with maximum gain. Assume V_{CC} = 1.8 V, I_C = 0.2 mA, I_S = 5 x 10-17 A, and β = 100.

Solution

Illustrated in Fig. 5.63(a), the circuit must operate properly with an input level of 600 mV. Thus, $V_b = V_{BE} + 600\text{mV} = V_T \ln(I_C/I_S) + 600\text{mV} = 1.354$ V. To avoid saturation, the collector voltage must not fall below the base voltage, thereby allowing a maximum voltage drop across R_C equal to 1.8V - 1.354V = 0.446V. We can then write

$$A_v = g_m R_C = \frac{I_C R_C}{V_T} = 17.2.$$

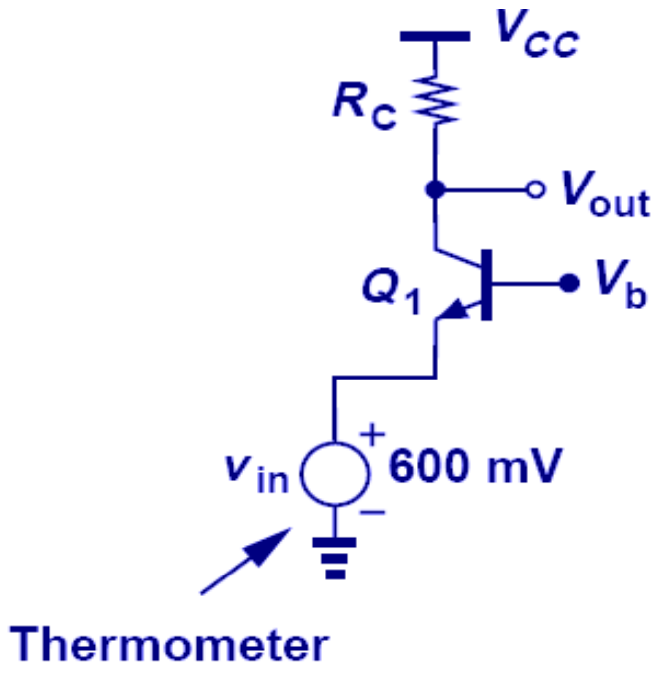
The reader is encouraged to repeat the problem with I_C = 0.4 mA to verify that the maximum gain remains relatively independent of the bias current.

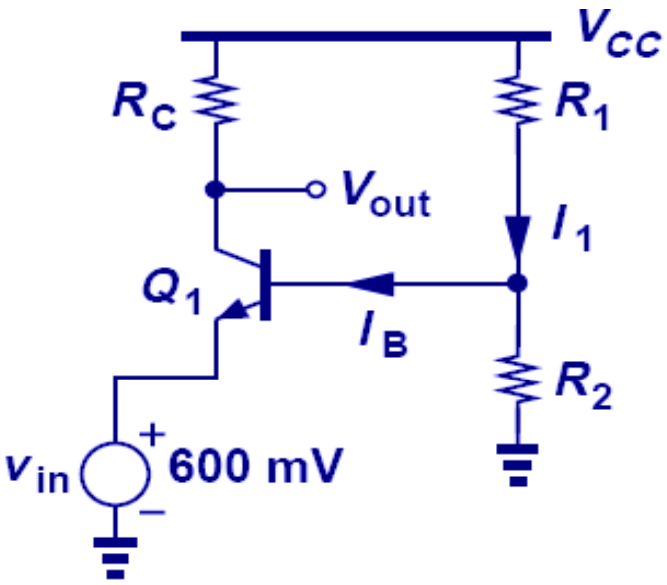
Example 5.35 (cnt'd)

We must now generate V_b. A simple approach is to employ a resistive divider as depicted in Fig. 5.63(b). To lower sensitivity to β, we choose $I_1 \approx 10I_B \approx 20\mu A \approx V_{CC}/(R_1+R_2)$. Thus, $R_1+R_2 = 90\ k\Omega$. Also,

$$V_b \approx \frac{R_2}{R_1+R_2}V_{CC} \quad \Longrightarrow \quad R_1 = 22.3k\Omega. \quad R_2 = 67.7k\Omega$$

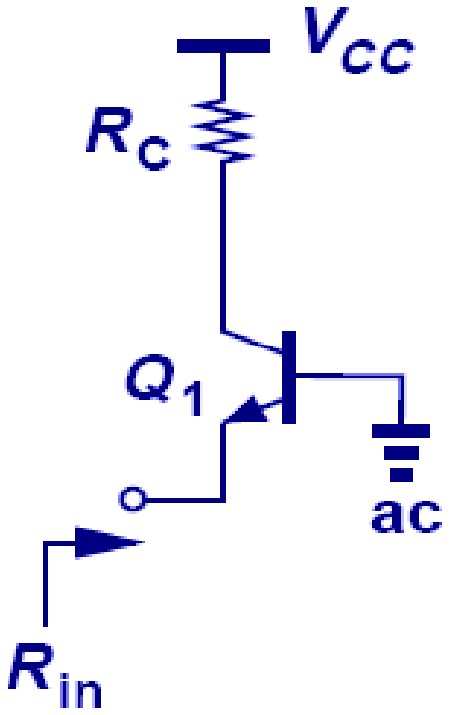
This example serves only as an illustration of the CB stage. A CE stage may prove more suited to sensing a thermometer voltage.

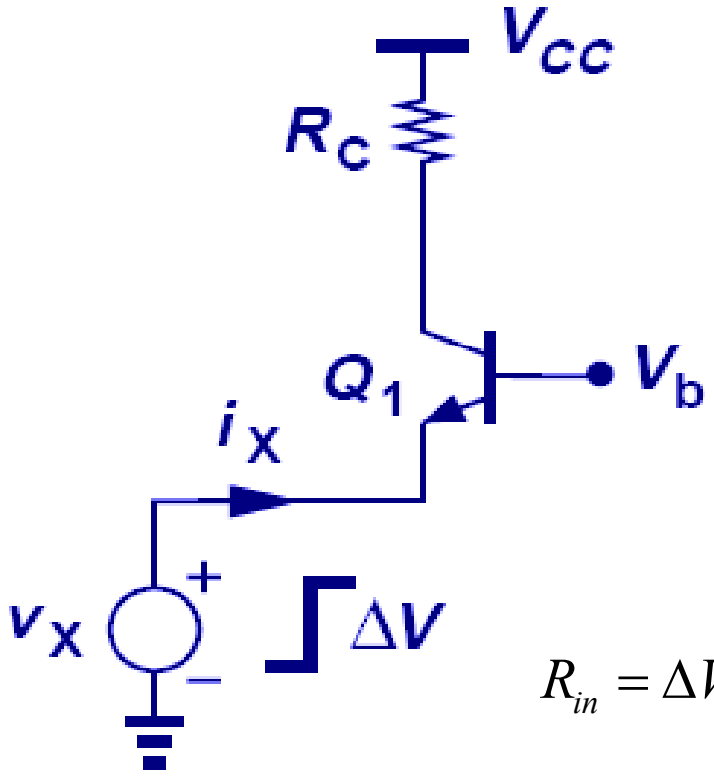




Input Impedance of CB

- The input impedance of CB stage, simply the impedance seen looking into the emitter with the base at ac ground, is much smaller than that of the CE stage.





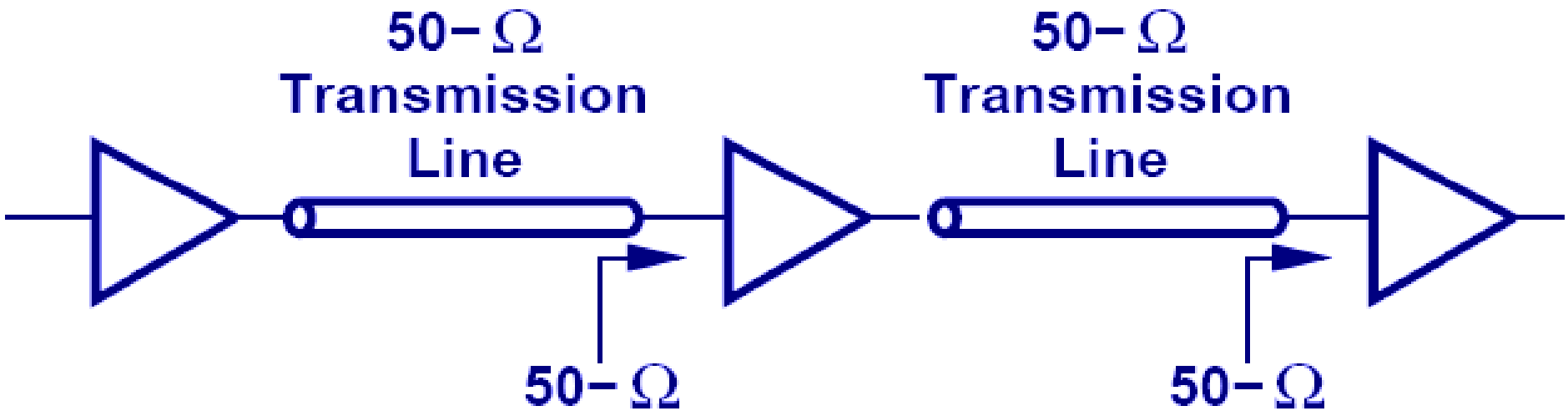
$$R_{in} = \Delta V_X / \Delta I_X = 1/g_m$$

$$R_{in} = \frac{1}{g_m}$$

relatively *low*, e.g., 26 Ω for $I_C = 1$ mA

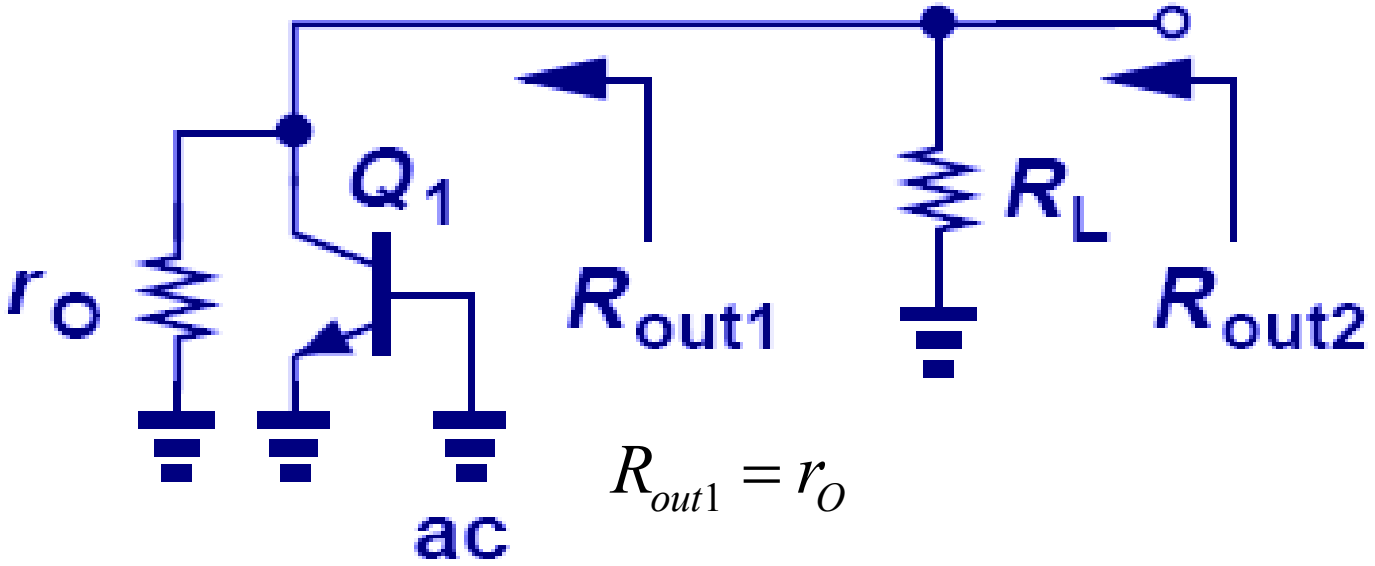
Practical Application of CB Stage

- To avoid "*reflection*," impedance matching is needed for interconnection.
- CB stage's low input impedance can be used to create a match with 50 Ω.



Output Impedance of CB Stage

- The output impedance of CB stage is similar to that of CE stage.



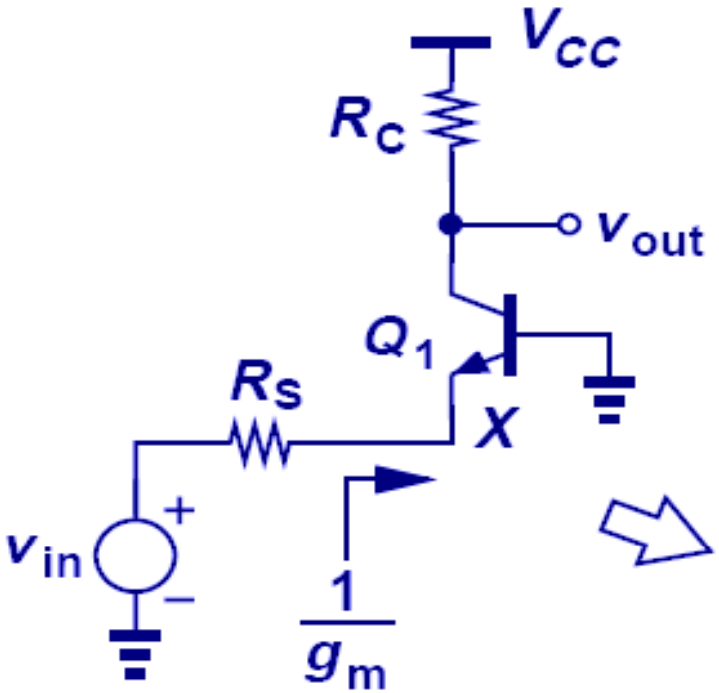
$$R_{out1} = r_O$$

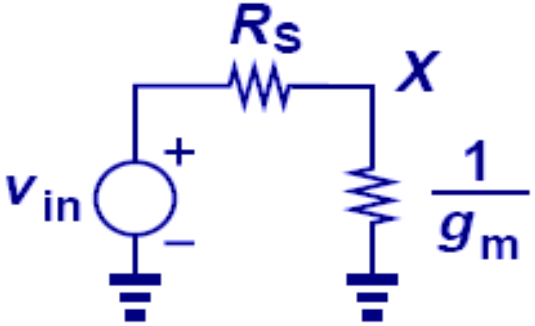
$$R_{out} = r_O \| R_C$$

$$= R_C \quad \text{if } V_A = \infty$$

CB Stage with Source Resistance

- With an inclusion of a source resistor, R_S, the input signal is attenuated before it reaches the emitter of the amplifier; therefore, we see a lower voltage gain.
- This is similar to CE stage emitter degeneration; only the phase is reversed.





$$v_X = \frac{\frac{1}{g_m}}{R_S + \frac{1}{g_m}} v_{in} = \frac{1}{1 + g_m R_S} v_{in}. \qquad \frac{v_{out}}{v_X} = g_m R_C.$$

$$\frac{v_{out}}{v_{in}} = \frac{g_m R_C}{1 + g_m R_S}$$

$$= \frac{R_C}{\frac{1}{g_m} + R_S},$$

Example 5.37

A common-base stage is designed to amplify an RF signal received by a 50-Ω antenna. Determine the required bias current if the input impedance of the amplifier must "match" the impedance of the antenna. What is the voltage gain if the CB stage also *drives* a 50-Ω load? Assume $V_A = \infty$.

Solution

Figure 5.68 depicts the amplifier and the equivalent circuit with the antenna modeled by a voltage source, v_{in}, and a resistance, $R_S = 50\Omega$. For impedance matching, it is necessary that the input impedance of the CB core, $1/g_m$, be equal to R_S, and hence $I_C = g_m V_T = 0.52$ mA.

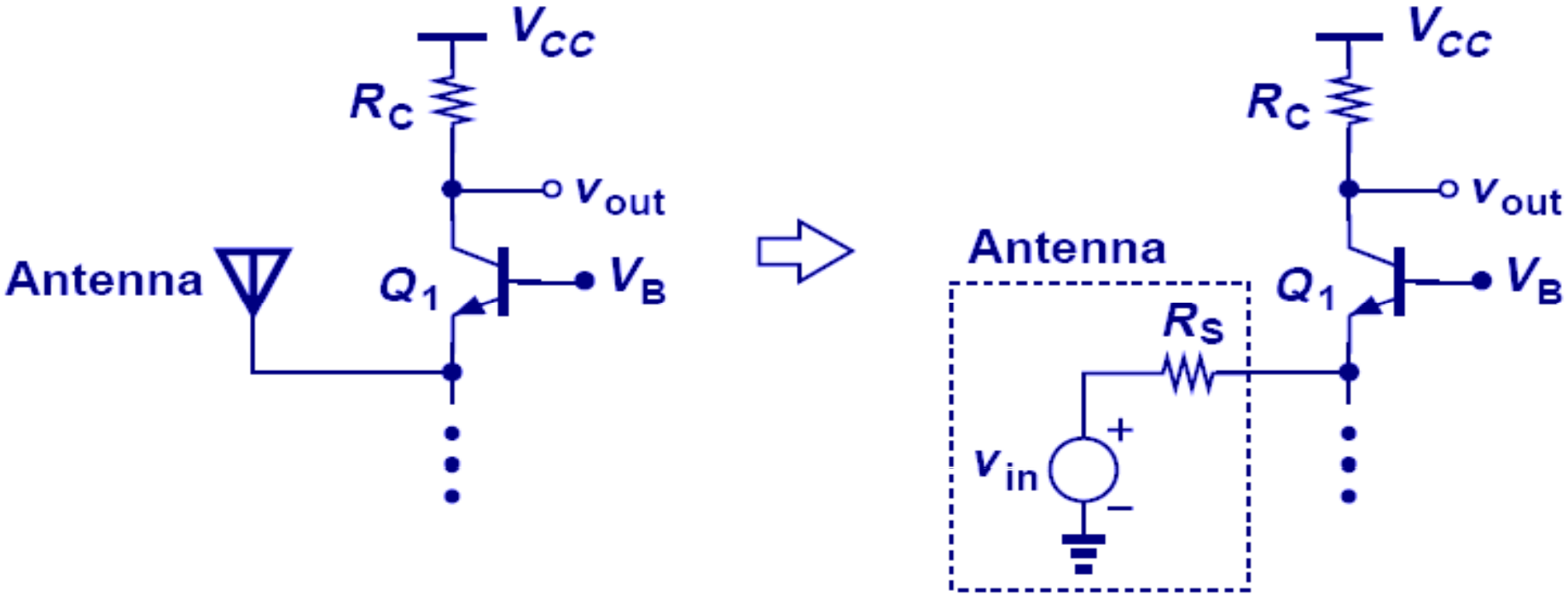
If R_C itself is replaced by a 50-Ω load, then Eq. (5.271) reveals that

$$A_v = \frac{R_C}{\frac{1}{g_m} + R_S} = \frac{1}{2}.$$

The circuit is therefore not suited to driving a 50-Ω load directly.

An antenna usually has low output impedance; therefore, a correspondingly low input impedance is required for the following stage.

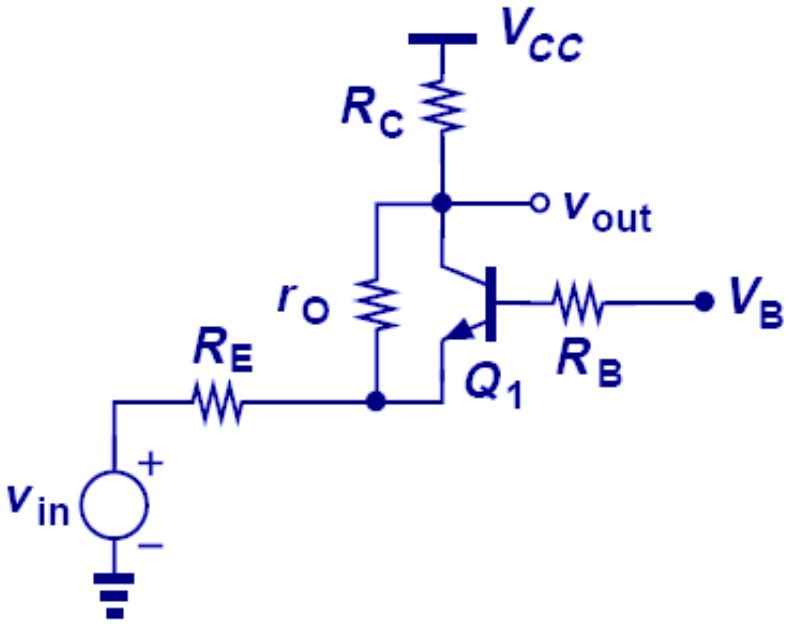
Example 5.37 CB Stage Applied at Antenna

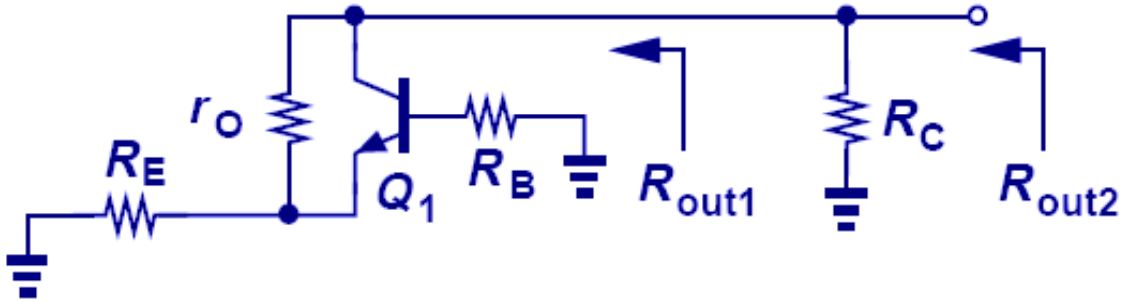


- The CB stage displays a current gain of *unity* because the current flowing into the emitter simply emerges from the collector (if the base current is neglected).
- On the other hand, for CE stage, $A_I = \beta$.

Realistic Output Impedance of CB Stage

- The output impedance of CB stage is equal to R_C in parallel with the impedance looking down into the collector.



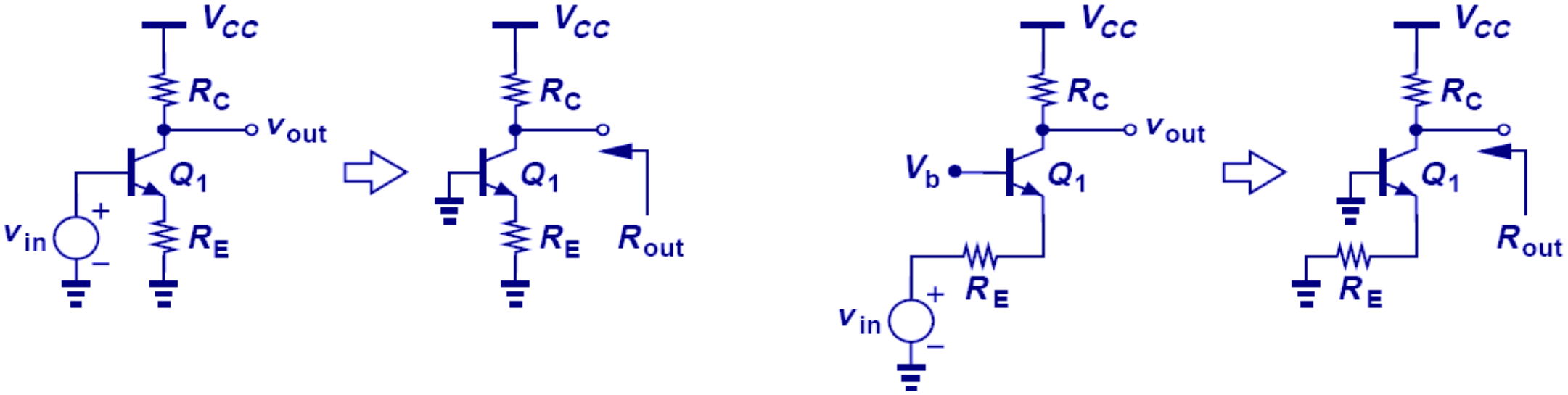


$$R_{out\,1} = \left[1 + g_m \left(R_E \parallel r_\pi\right)\right] r_O + \left(R_E \parallel r_\pi\right)$$

$$R_{out} = R_C \parallel R_{out\,1}$$

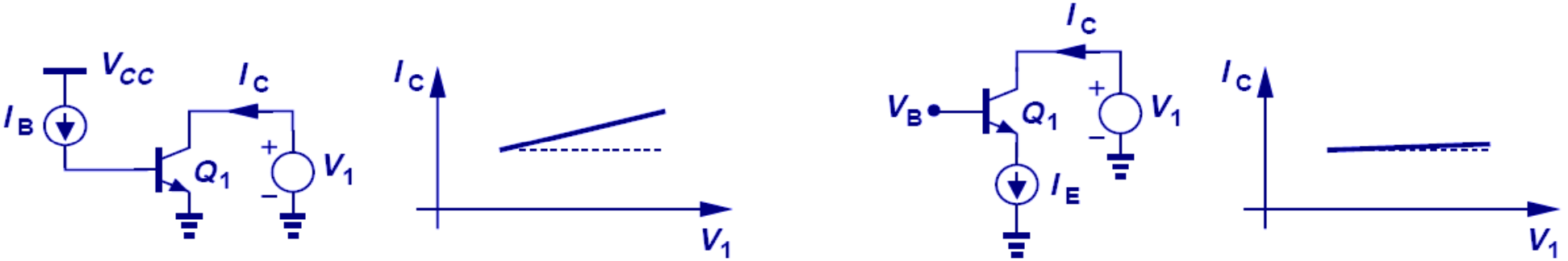
Output Impedance of CE and CB Stages

- The output impedances of CE, CB stages are the same if both circuits are under the same condition.
- This is because when calculating output impedance, the input port is grounded, which renders the same circuit for both CE and CB stages.



Fallacy of the "Old Wisdom"

- The statement "CB output impedance is higher than CE output impedance" is flawed.
- As illustrated in Fig. 5.71, a constant current is injected into the base while the collector voltage is varied, I_C exhibits a slope equal to r_O^{-1} [Fig. 5.71(a)]. On the other hand, if a constant current is drawn from the emitter, displays much less dependence on the collector voltage.
- In practice, however, each stage may be driven by a *voltage* source having a finite impedance, making the above comparison irrelevant.



CB with Base Resistance

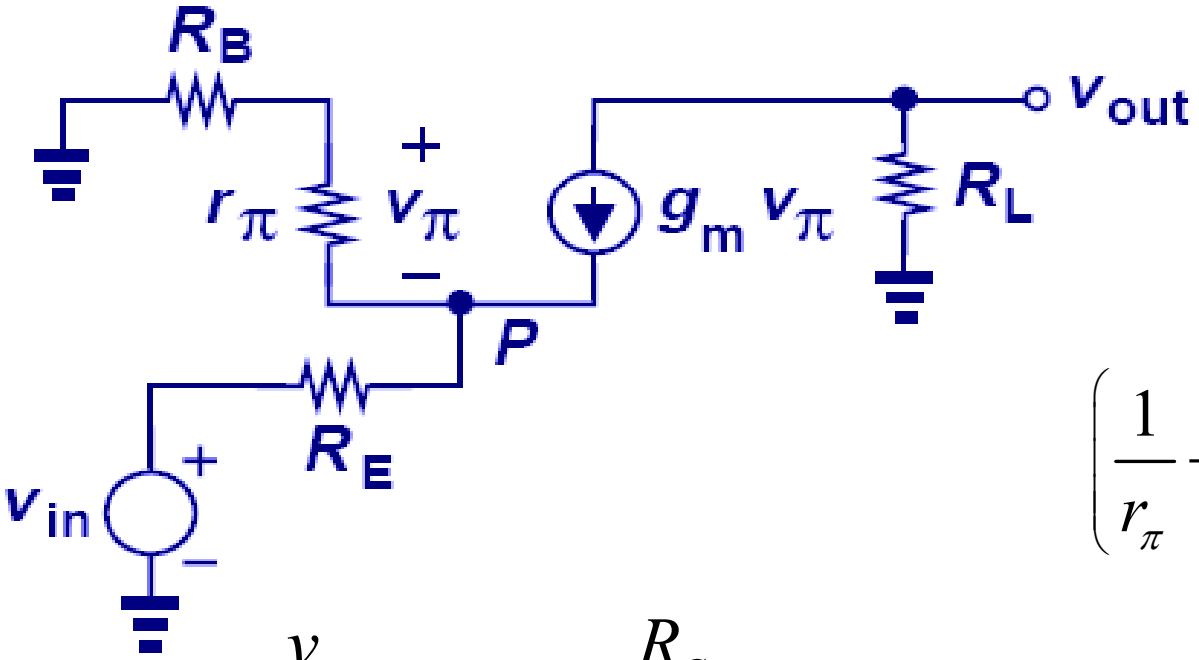
- With an addition of base resistance, R_B, the voltage gain degrades.

$$g_m v_\pi = -v_{out}/R_C \qquad v_\pi = -v_{out}/(g_m R_C)$$

$$v_\pi/r_\pi = -v_{out}/(g_m r_\pi R_C) = -v_{out}/(\beta R_C)$$

$$v_P = -\frac{-v_{out}}{\beta R_C}(R_B + r_\pi)$$

$$= \frac{v_{out}}{\beta R_C}(R_B + r_\pi).$$



$$\frac{v_\pi}{r_\pi} + g_m v_\pi = \frac{v_P - v_{in}}{R_E};$$

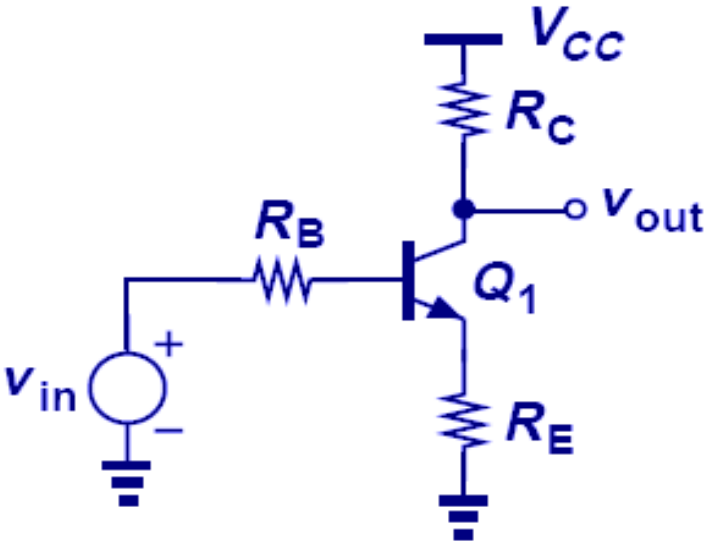
$$\left(\frac{1}{r_\pi} + g_m\right)\frac{-v_{out}}{g_m R_C} = \frac{\frac{v_{out}}{\beta R_C}(R_B + r_\pi) - v_{in}}{R_E}.$$

$$\frac{v_{out}}{v_{in}} \approx \frac{R_C}{R_E + \frac{R_B}{\beta+1} + \frac{1}{g_m}}$$

$$\frac{v_{out}}{v_{in}} = \frac{\beta R_C}{(\beta+1)R_E + R_B + r_\pi}.$$

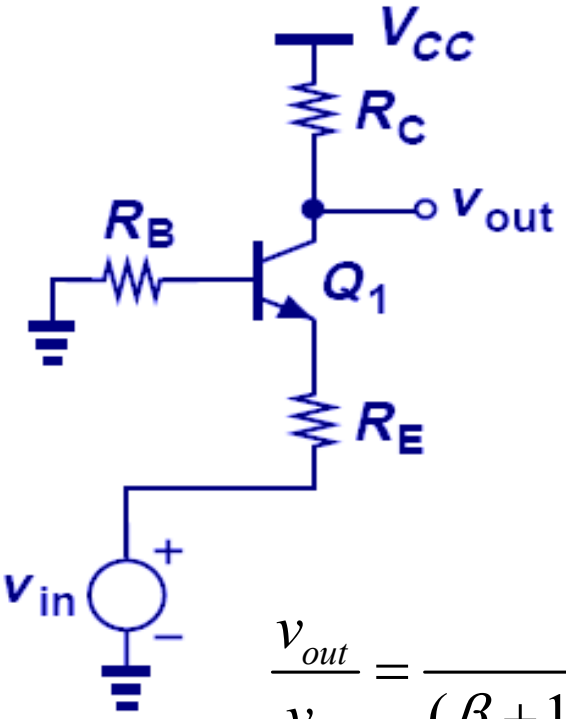
Comparison of CE and CB Stages with R_B

- The voltage gain of CB amplifier with base resistance is exactly the same as that of CE stage with base resistance and emitter degeneration, except for a negative sign.



$$\frac{v_{out}}{v_{in}} = \frac{-\beta R_C}{r_\pi + (\beta+1)R_E + R_B}$$

$$A_v \approx \frac{-R_C}{\frac{1}{g_m} + R_E + \frac{R_B}{\beta+1}}$$

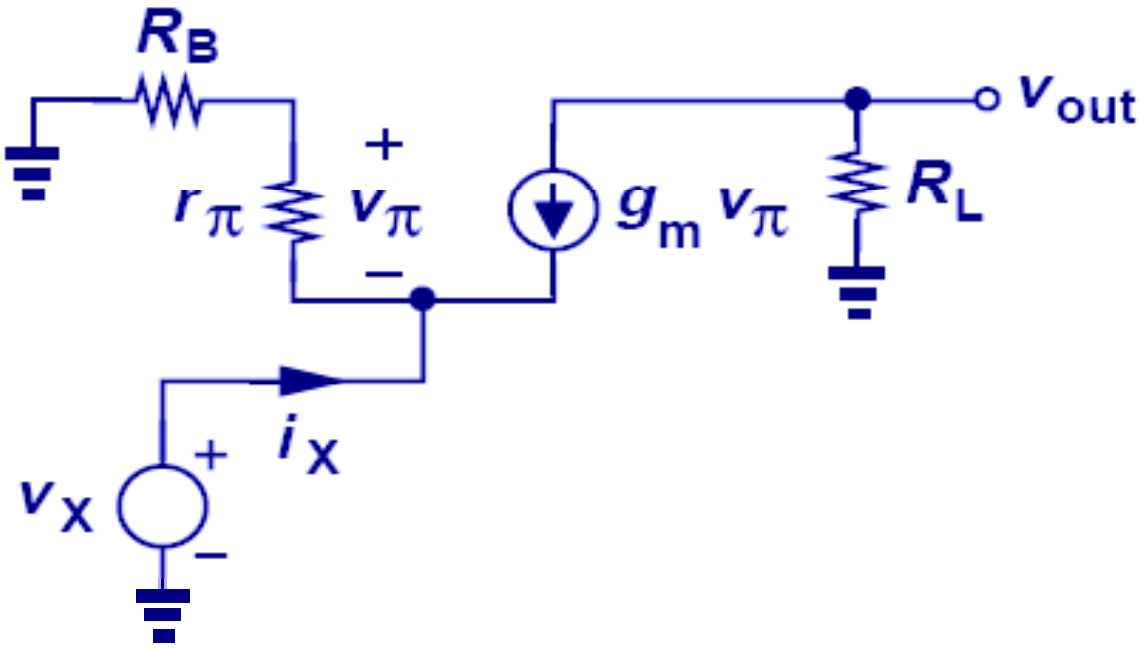


$$\frac{v_{out}}{v_{in}} = \frac{\beta R_C}{(\beta+1)R_E + R_B + r_\pi}.$$

$$\frac{v_{out}}{v_{in}} \approx \frac{R_C}{R_E + \frac{R_B}{\beta+1} + \frac{1}{g_m}}$$

Input Impedance of CB Stage with R_B

- The input impedance of CB with R_B is equal to $1/g_m$ plus R_B divided by (β+1).
- This is in contrast to degenerated CE stage, in which the resistance in series with the emitter is *multiplied* by (β+1) when seen from the base.



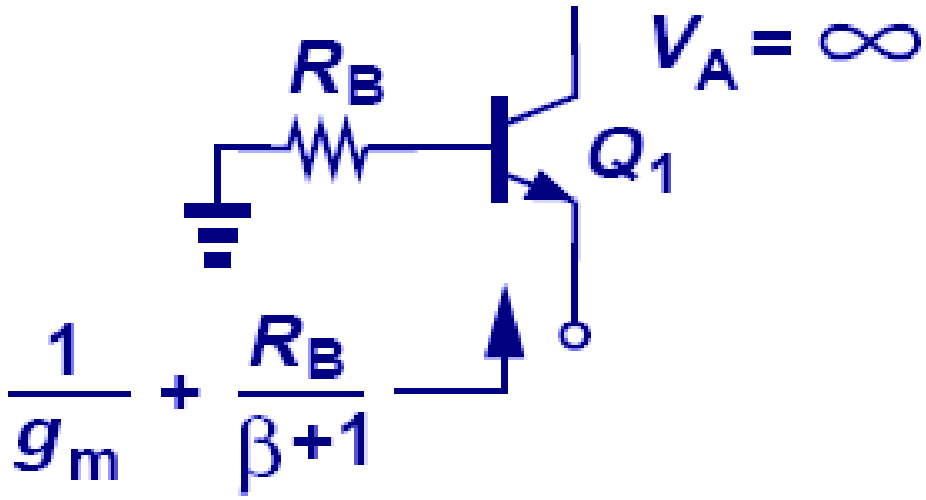
$$v_\pi = -\frac{r_\pi}{r_\pi + R_B} v_X .$$

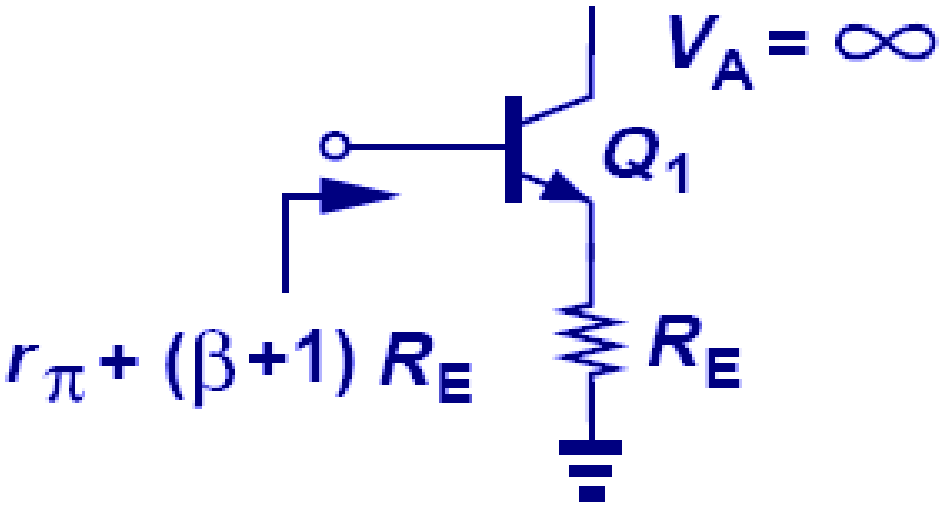
$$\frac{v_\pi}{r_\pi} + g_m v_\pi = -i_X .$$

$$\left(\frac{1}{r_\pi} + g_m\right)\frac{-r_\pi}{r_\pi + R_B} v_X = -i_X$$

$$\frac{v_X}{i_X} = \frac{r_\pi + R_B}{\beta + 1} \approx \frac{1}{g_m} + \frac{R_B}{\beta + 1}$$

Input Impedance Seen at Emitter and Base





Example 5.39

Determine the impedance seen at the emitter of Q_2 in Fig. 5.76(a) if the two transistors are identical and $V_A = \infty$.

Solution

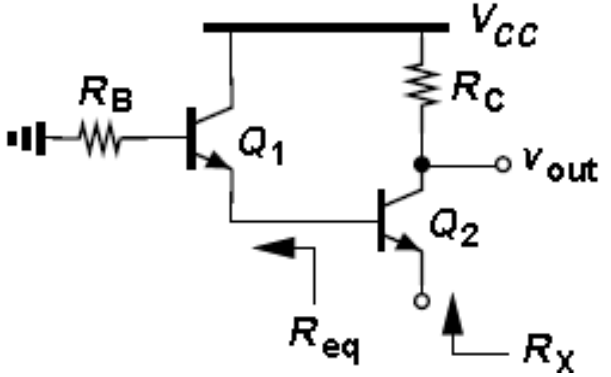
The circuit employs Q_2 as a common-base device, but with its base tied to a finite series resistance equal to that seen at the emitter of Q_1. Thus, we must first obtain the equivalent resistance R_{eq}, which from Eq. (5.291) is simply equal to

$$R_{eq} = \frac{1}{g_{m1}} + \frac{R_B}{\beta + 1}.$$

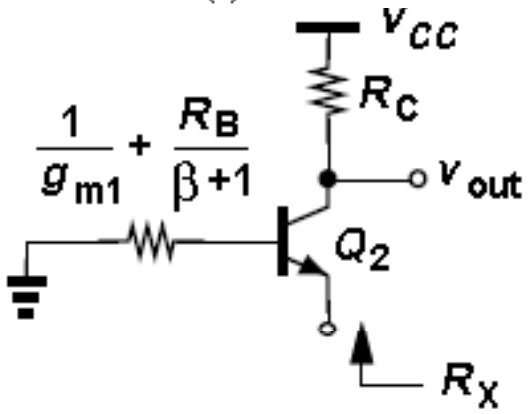
Reducing the circuit to that shown in Fig. 5.76(b), we have

$$R_X = \frac{1}{g_{m2}} + \frac{R_{eq}}{\beta + 1}$$

$$= \frac{1}{g_{m2}} + \frac{1}{\beta + 1}\left(\frac{1}{g_{m1}} + \frac{R_B}{\beta + 1}\right).$$



(a)



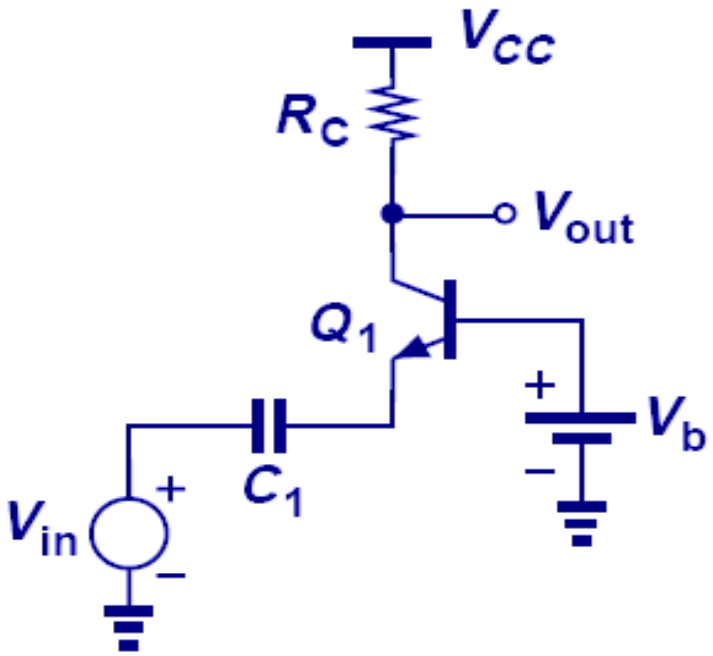
(b)

Example 5.40 bad CB biasing

The student in Example 5.31 decides to incorporate ac coupling at the input of a CB stage to ensure the bias is not affected by the signal source, drawing the design as shown in Fig. 5.77. Explain why this circuit does not work.

Solution

Unfortunately, the design provides no dc path for the emitter current of Q_1, forcing a zero bias current and hence a zero transconductance. The situation is similar to the CE counterpart in Example 5.5, where no base current can be supported.

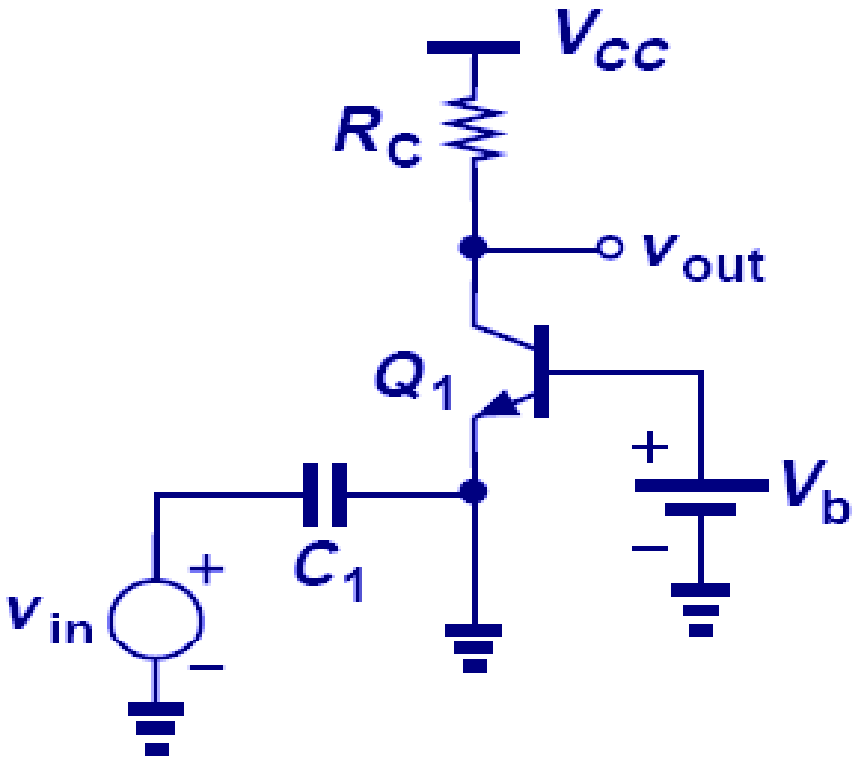


Example 5.41 Still No Good

Somewhat embarrassed, the student quickly connects the emitter to ground so that $V_{BE} = V_b$ and a reasonable collector current can be established (Fig. 5.78). Explain why "haste makes waste."

Solution

As with Example 5.6, the student has shorted the *signal* to ac ground. That is, the emitter voltage is equal to zero regardless of the value of v_{in}, yielding $v_{out} = 0$.



Proper Biasing for CB Stage

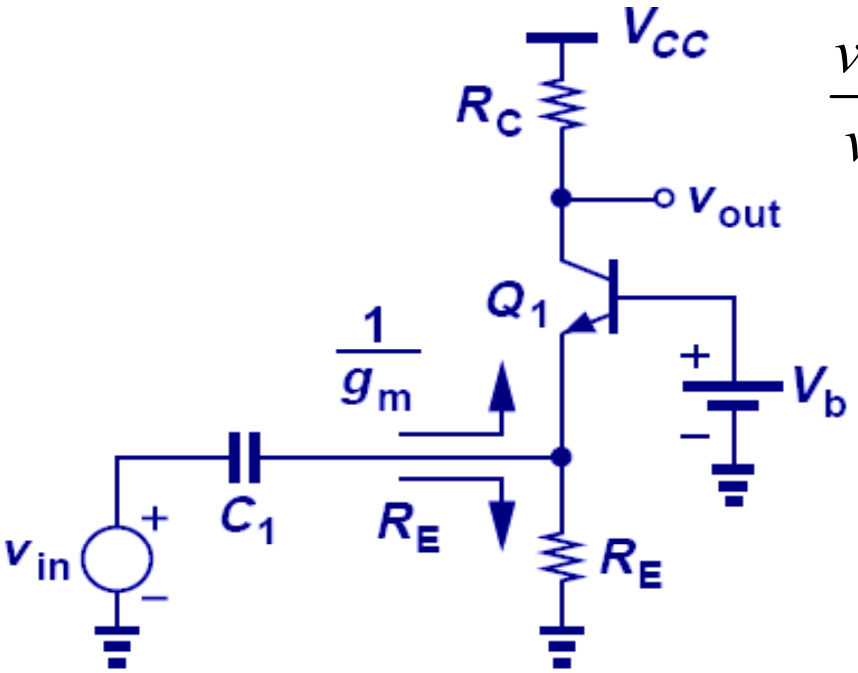
- R_E provides a path for the bias current at the cost of lowering the input impedance.
- R_{in} now consists of two *parallel* components: (1) $1/g_m$, seen looking "up" into the emitter (with the base at ac ground) and (2) R_E, seen looking "down."

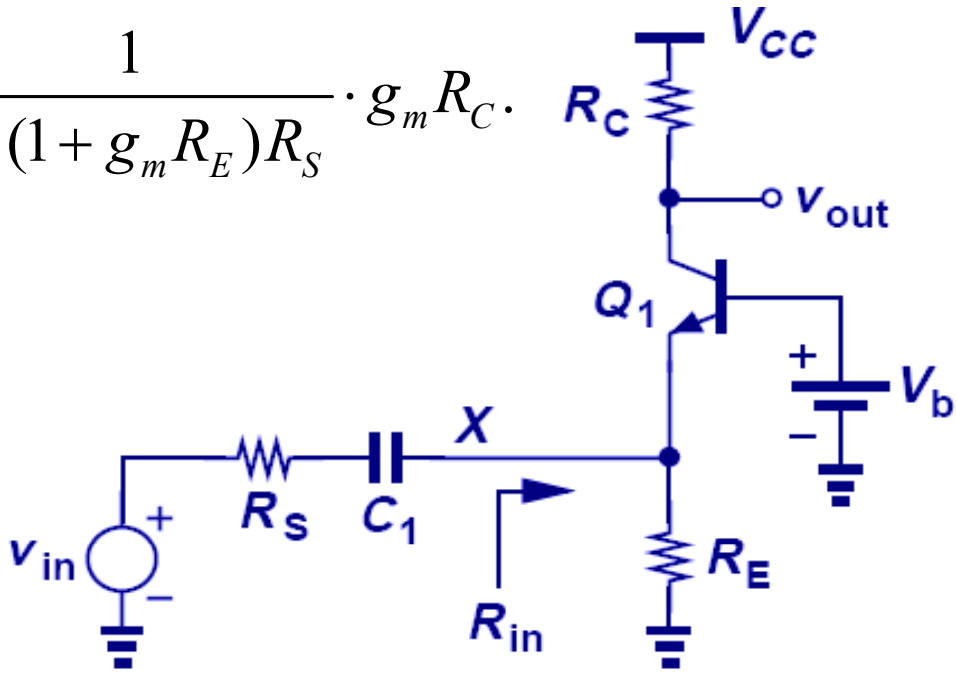
$$R_{in} = \frac{1}{g_m} \| R_E .$$

$$\frac{v_X}{v_{in}} = \frac{R_{in}}{R_{in} + R_S} = \frac{\frac{1}{g_m} \| R_E}{\frac{1}{g_m} \| R_E + R_S} = \frac{1}{1 + (1 + g_m R_E) R_S} .$$

$$v_{out}/v_X = g_m R_C$$

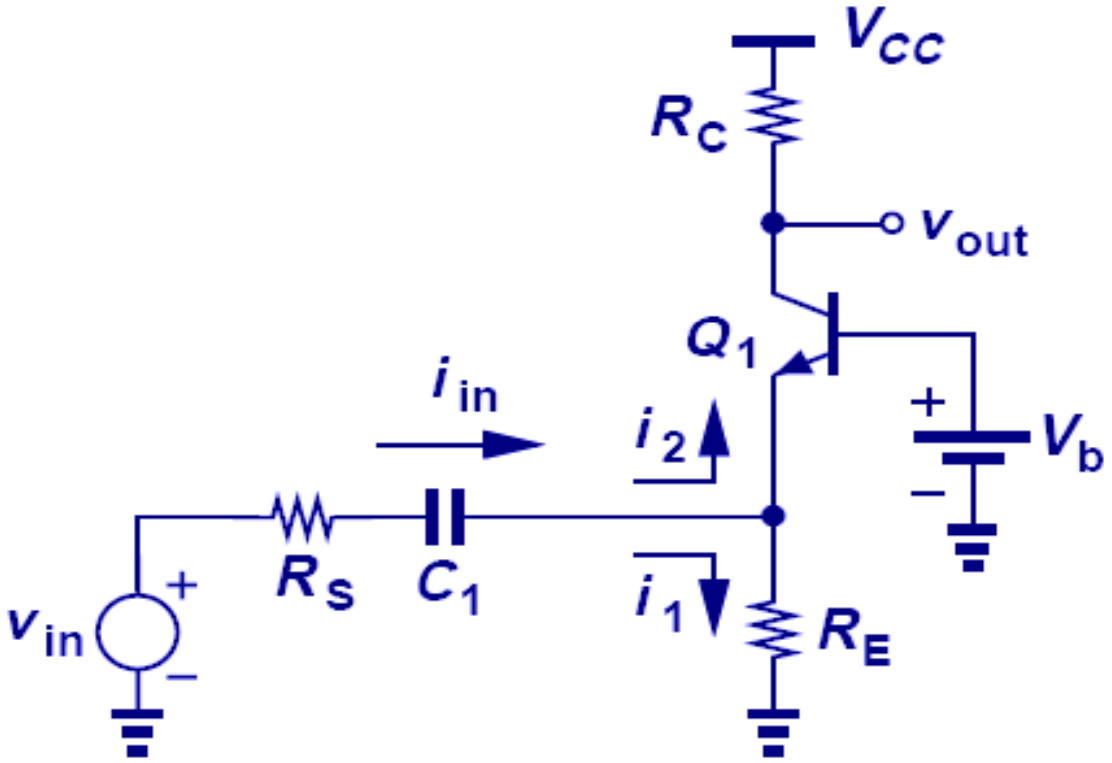
$$\frac{v_{out}}{v_{in}} = \frac{1}{1 + (1 + g_m R_E) R_S} \cdot g_m R_C .$$





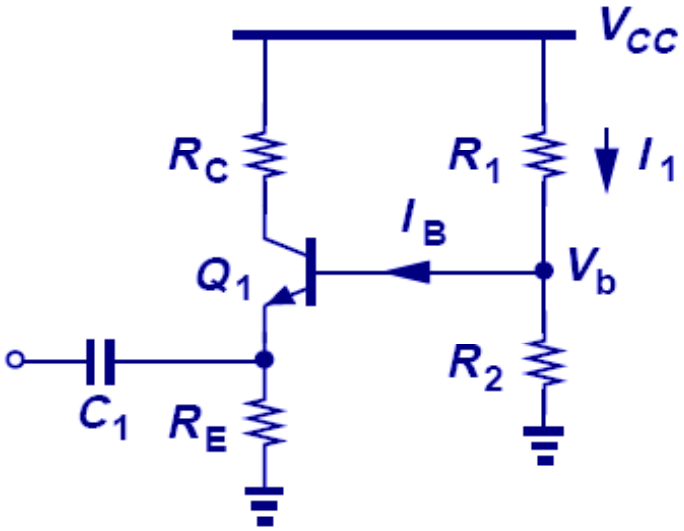
Reduction of Input Impedance Due to R_E

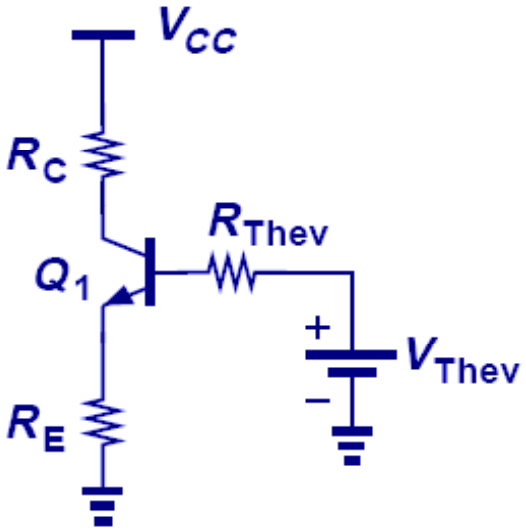
- The reduction of input impedance due to R_E is bad because it shunts part of the input current, i_1, to ground instead of to Q_1 (and R_C).
- For R_E to affect the input impedance negligibly, we must have $R_E >> 1/g_m$, and hence $I_C R_E >> V_T$
- That is, the dc voltage drop across R_E must be much greater than V_T.

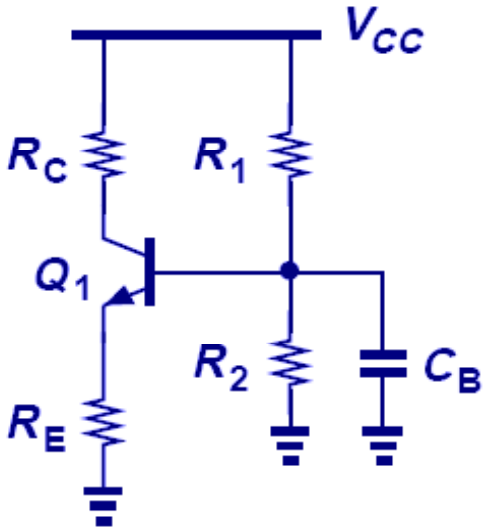


Creation of V_b

- Resistive divider lowers the gain.
- To remedy this problem, a '***bypass capacitor,*** C_B' is inserted from base to ground to short out the resistor divider at the frequency of interest.







ensure $I_1 >> I_B$ to minimize sensitivity to β, so $V_b \approx \dfrac{R_2}{R_1 + R_2} V_{CC}$.

Example 5.42

Design a CB stage (Fig. 5.82) for a voltage gain of 10 and an input impedance of 50 Ω. Assume $I_S = 5\text{x}10^{-16}$ A, $V_A = \infty$, $\beta = 100$, and $V_{CC} = 2.5$ V.

Solution

We begin by selecting $R_E >> 1/g_m$, e.g., $R_E = 500\ \Omega$, to minimize the undesirable effect of R_E. Thus,

$$R_{in} \approx \frac{1}{g_m} = 50\Omega$$

and hence

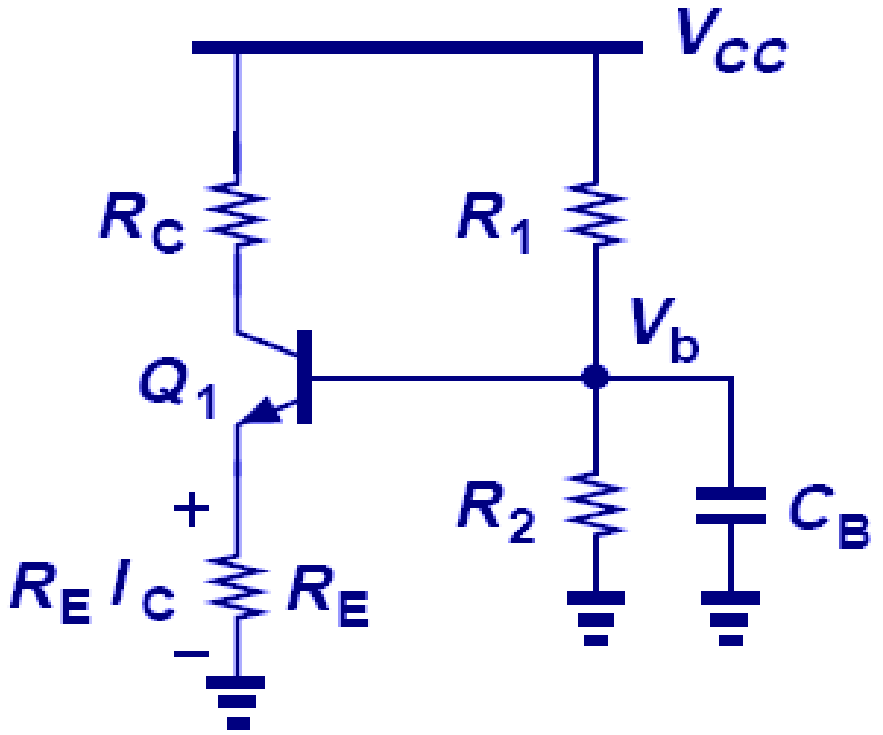
$$I_C = 0.52\text{mA}.$$

If the base is bypassed to ground

$$A_v = g_m R_C,$$

yielding

$$R_C = 500\Omega.$$



$$\frac{v_{out}}{v_{in}} \approx \frac{R_C}{R_E + \frac{R_B}{\beta+1} + \frac{1}{g_m}}$$

Example 5.42 (cnt'd)

We now determine the base bias resistors. Since the voltage drop across R_E is equal to 500 Ω x 0.52 mA = 260 mV and $V_{BE} = V_T \ln(I_C/I_S) = 899$ mV, we have

$$V_b = I_E R_E + V_{BE} = 1.16\text{V}.$$

Selecting the current through R_1 and R_2 to be $10I_B = 52$ μA, we write

$$V_b \approx \frac{R_2}{R_1 + R_2} V_{CC}. \qquad \frac{V_{CC}}{R_1 + R_2} = 52\mu\text{A}.$$

It follows that

$$R_1 = 25.8\text{k}\Omega \qquad R_2 = 22.3\text{k}\Omega.$$

The last step in the design is to compute the required values of C_1 and C_B according to the signal frequency. For example, if the amplifier is used at the receiver front end of a 900-MHz cellphone, the impedances of C_1 and C_B must be sufficiently small at this frequency. Appearing in series with the emitter of Q_1, C_1 plays a role similar to R_S in Fig. 5.67 and Eq. (5.271). Thus, its impedance, $|C_1\omega|^{-1}$, must remain much less than $1/g_m = 50$ Ω. In high-performance applications such as cellphones, we may choose $|C_1\omega|^{-1} = (1/g_m)/20$ to ensure negligible gain degradation.

Example 5.42 (cnt'd)

Consequently, for $\omega = 2\pi$ x 900 MHz:

$$C_1 = \frac{20 g_m}{\omega} = 71\text{pF}.$$

Since the impedance of C_B appears in series with the base and plays a role similar to the term $R_B/(\beta+1)$ in Eq. (5.286), we require that

$$\frac{1}{\beta+1}\left|\frac{1}{C_B\omega}\right| = \frac{1}{20}\frac{1}{g_m}$$

$$\frac{v_{out}}{v_{in}} \approx \frac{R_C}{R_E + \dfrac{R_B}{\beta+1} + \dfrac{1}{g_m}}$$

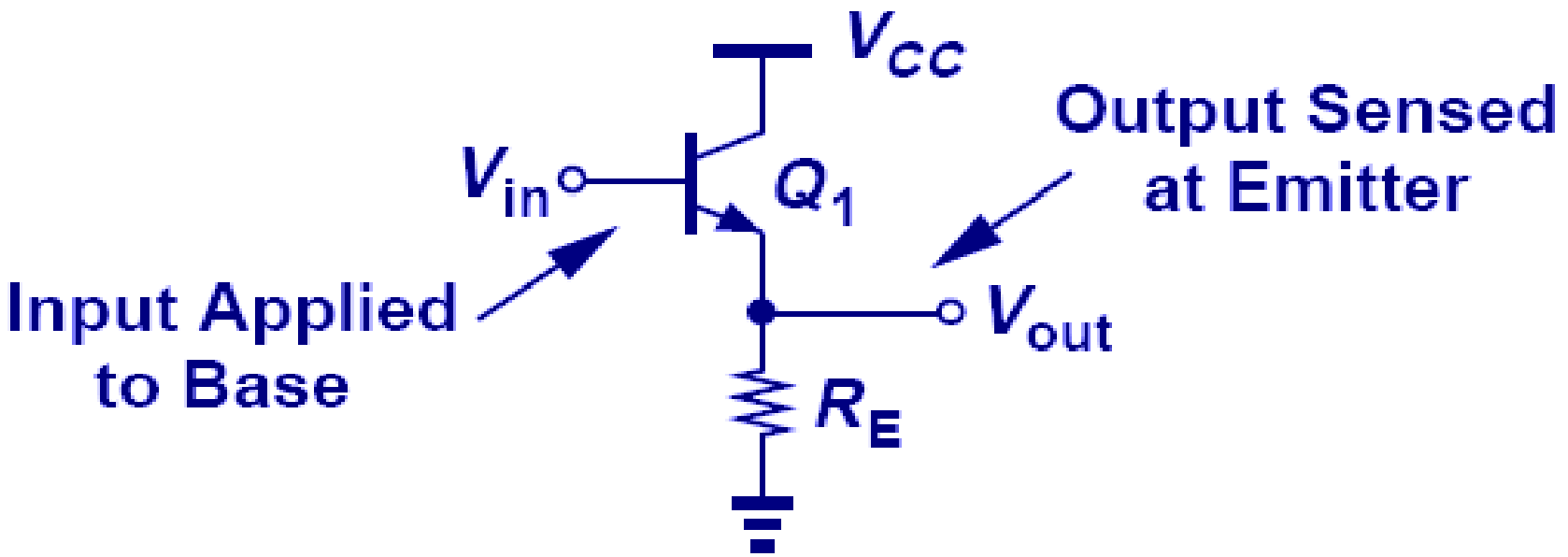
and hence

$$C_B = 0.7\text{pF}.$$

(A common mistake is to make the impedance of C_B negligible with respect to $R_1 \| R_2$ rather than with respect to $1/g_m$.)

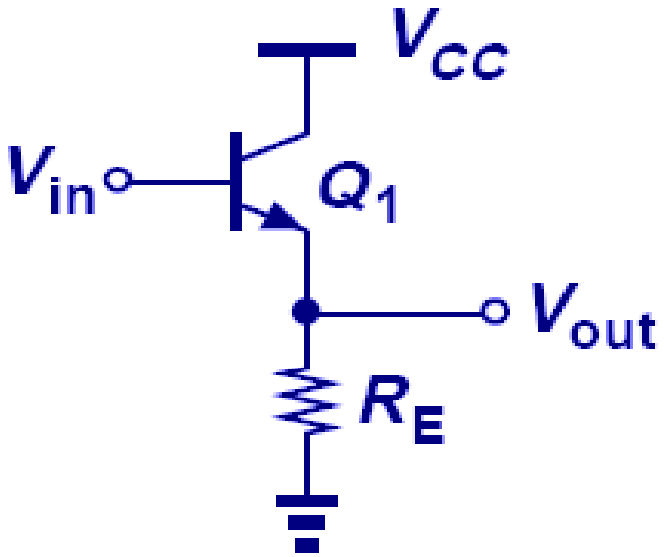
Emitter Follower (Common Collector Amplifier)

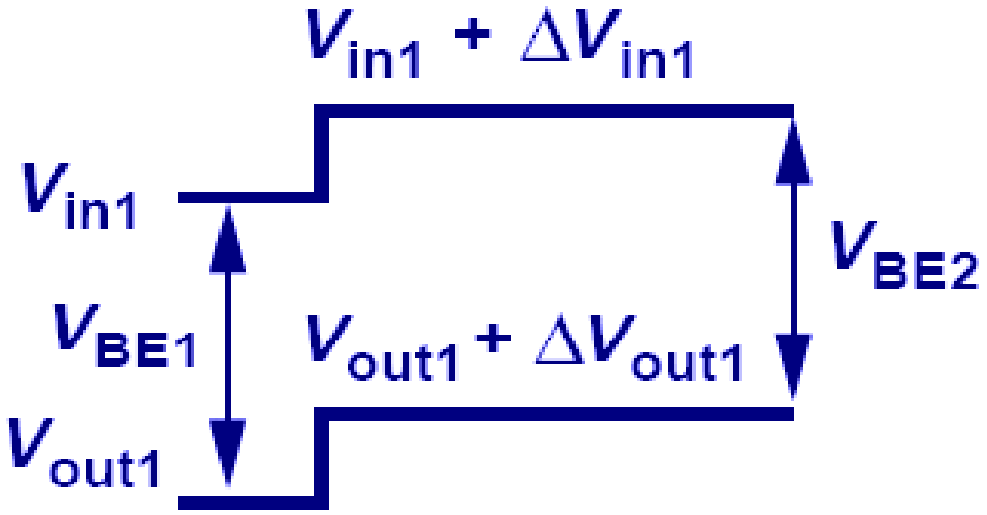
- The emitter follower senses the input at the base of the transistor and produces the output at the emitter. The collector is tied to V_{CC} and hence ac ground.



Emitter Follower Core

- When the input is increased by ΔV, output is also increased by an amount that is less than ΔV due to the increase in collector current and hence the increase in potential drop across R_E.
- However the absolute values of input and output differ by a V_{BE}.
- V_{out} is always lower than V_{in} by an amount equal to V_{BE}, and the circuit is said to provide "***level shift***."
- $\Delta V_{out} < \Delta V_{in}$ implies that the follower exhibits a voltage gain less than unity.





$$\Delta V_{out} < \Delta V_{in} \qquad V_{BE2} > V_{BE1}$$

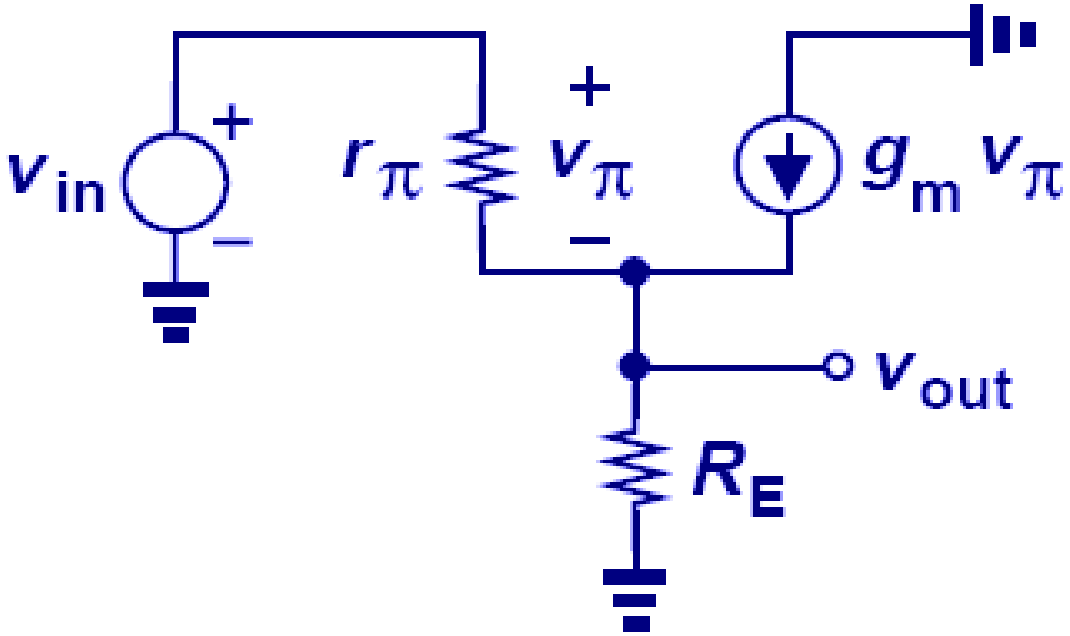
Small-Signal Model of Emitter Follower

- As shown, the voltage gain is less than unity and positive.

$$V_A = \infty$$

$$\frac{v_\pi}{r_\pi} + g_m v_\pi = \frac{v_{out}}{R_E} \qquad v_\pi = \frac{r_\pi}{\beta+1} \cdot \frac{v_{out}}{R_E}.$$

$$v_{in} = v_\pi + v_{out}. \qquad \frac{v_{out}}{v_{in}} = \frac{1}{1 + \frac{r_\pi}{\beta+1} \cdot \frac{1}{R_E}} \approx \frac{R_E}{R_E + \frac{1}{g_m}}.$$



Example 5.43 Unity-Gain Emitter Follower

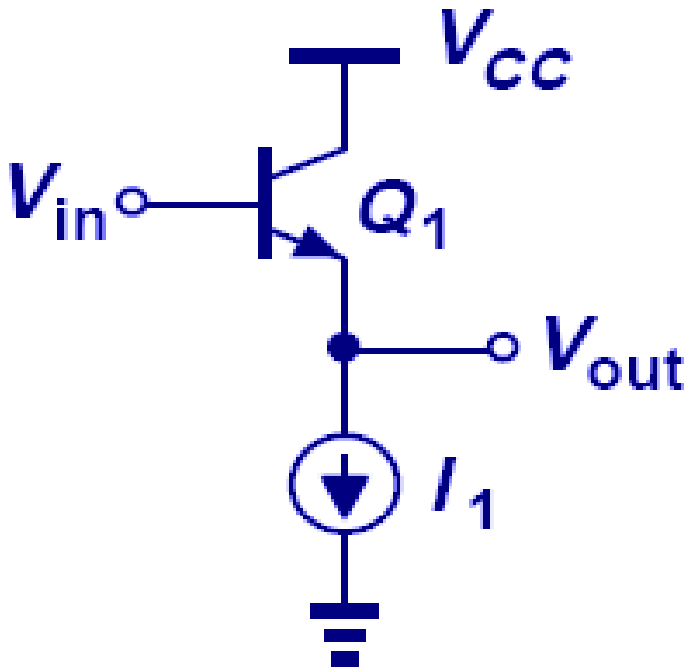
In integrated circuits, the follower is typically realized as shown in Fig. 5.86. Determine the voltage gain if the current source is ideal and $V_A = \infty$.

Solution

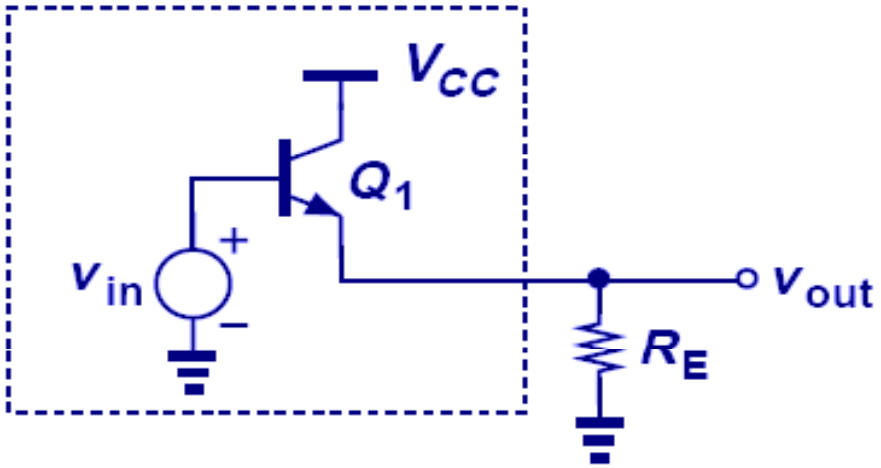
Since the emitter resistor is replaced with an ideal current source, the value of R_E in Eq. (5.321) must tend to infinity, yielding

$$A_v = 1$$

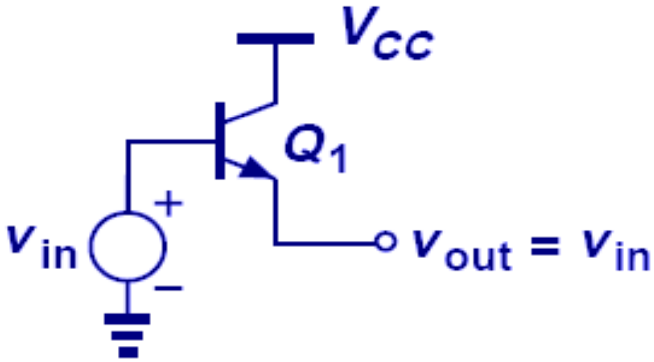
This result can also be derived intuitively.
A constant current source flowing through Q_1 requires that $V_{BE} = V_T \ln(I_C/I_S)$ remain constant.
Writing $V_{out} = V_{in} - V_{BE}$, we recognize that V_{out} exactly *follows* V_{in} if V_{BE} is constant.



Analysis of Emitter Follower as a Voltage Divider

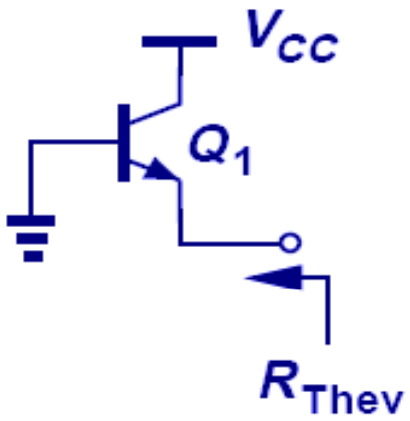


(a)

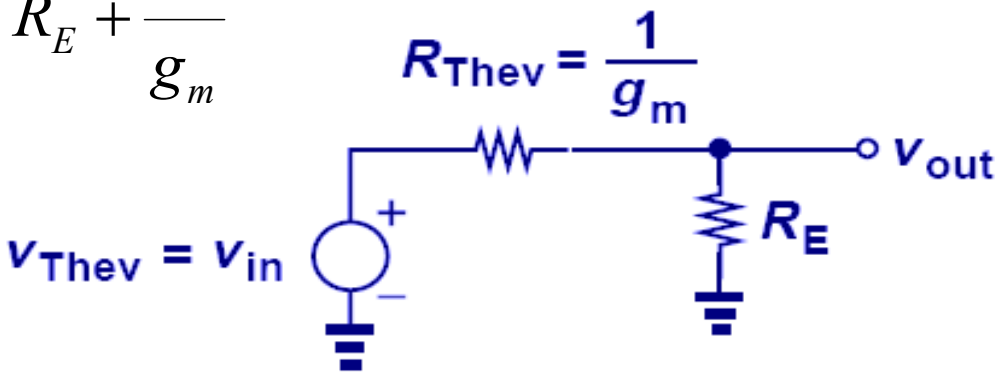


(b)

$$\frac{v_{out}}{v_{in}} \approx \frac{R_E}{R_E + \dfrac{1}{g_m}}.$$



(c)



(d)

Example 5.44 CC with R_S

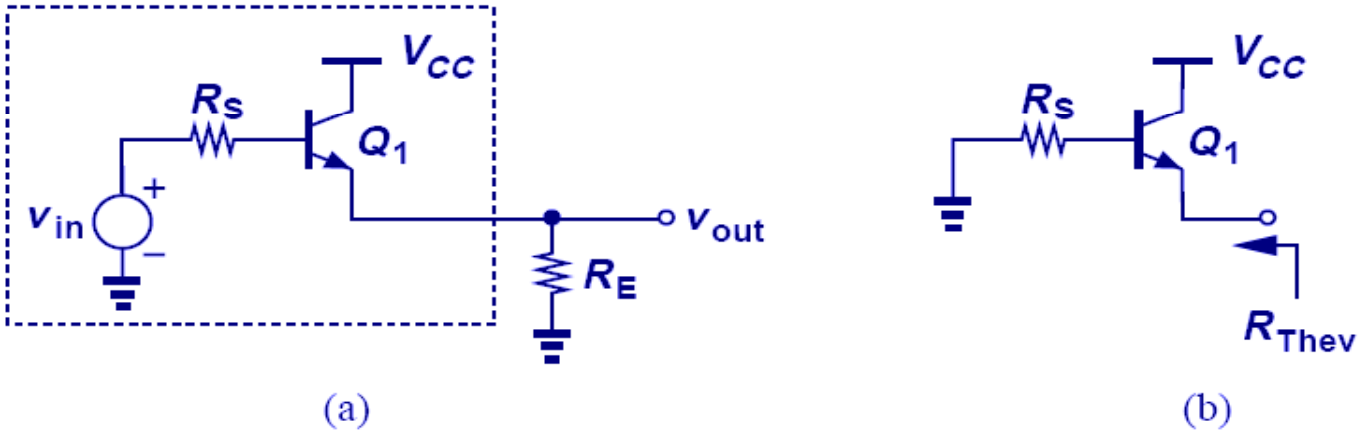
Determine the voltage gain of a follower driven by a finite source impedance of R_S [Fig. 5.88(a)] if $V_A = \infty$.

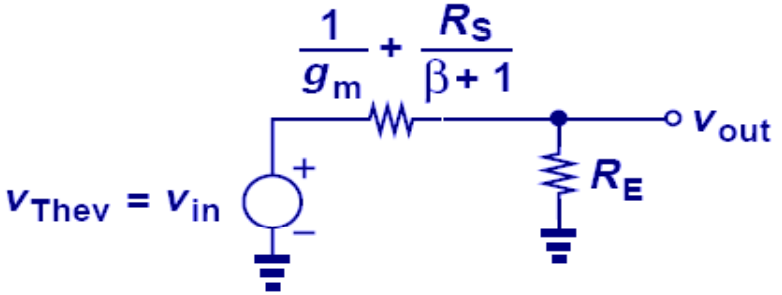
Solution

We model v_{in}, R_S, and Q_1 by a Thevenin equivalent. The reader can show that the open-circuit voltage is equal to v_{in}. Furthermore, the Thevenin resistance [Fig. 5.88(b)] is given by (5.291) as $R_S/(\beta+1) + 1/g_m$. Figure 5.88(c) depicts the equivalent circuit, revealing that

$$\frac{v_{out}}{v_{in}} = \frac{R_E}{R_E + \dfrac{R_S}{\beta+1} + \dfrac{1}{g_m}}.$$

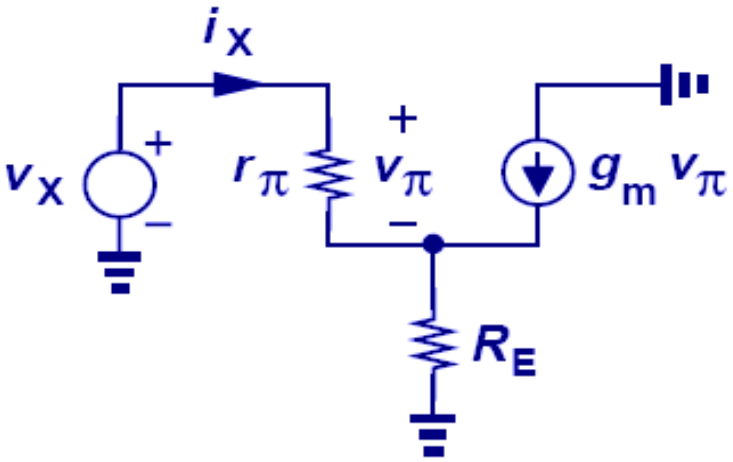
This result can also be obtained by solving the small-signal equivalent circuit of the follower.

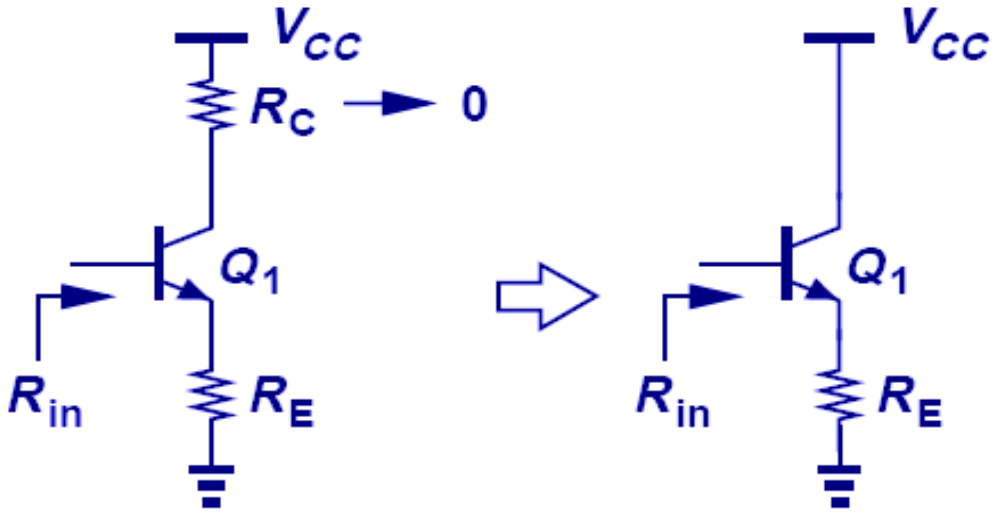




Input Impedance of Emitter Follower

- The input impedance of emitter follower is exactly the same as that of CE stage with emitter degeneration. This is not surprising because the input impedance of CE with emitter degeneration does not depend on the collector resistance.
- The follower "transforms" the load resistor, R_E, to a much larger value, thereby serving as an efficient "***buffer***."





$$v_X = v_\pi + (i_X + g_m v_\pi) R_E$$

$$= i_X r_\pi + (i_X + g_m i_X r_\pi) R_E,$$

$$\frac{v_X}{i_X} = r_\pi + (1+\beta) R_E.$$

Example 5.45 Emitter Follower as Buffer

A CE stage exhibits a voltage gain of 20 and an output resistance of 1 kΩ. Determine the voltage gain of the CE amplifier if (a) The stage drives an 8-Ω speaker directly. (b) An emitter follower biased at a current of 5 mA is interposed between the CE stage and the speaker. Assume β = 100, $V_A = \infty$, and the follower is biased with an ideal current source.

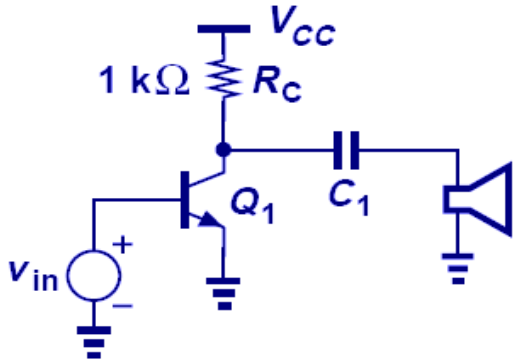
Solution

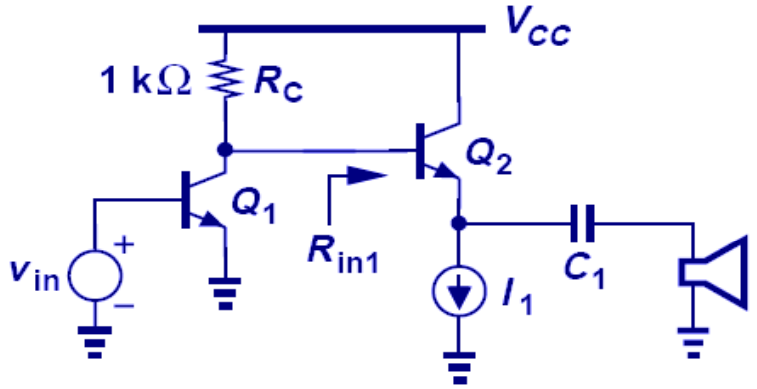
(a) As depicted in Fig. 5.90(a), the equivalent resistance seen at the collector is now given by the parallel combination of R_C and the speaker impedance, R_{SP}, reducing the gain from 20 to $20\text{x}(R_C||8\Omega)/R_C = 0.159$. The voltage gain therefore degrades drastically.

(b) From the arrangement in Fig. 5.90(b), we note that

$$R_{in1} = r_{\pi 2} + (\beta + 1)R_{sp} = 1058\Omega.$$

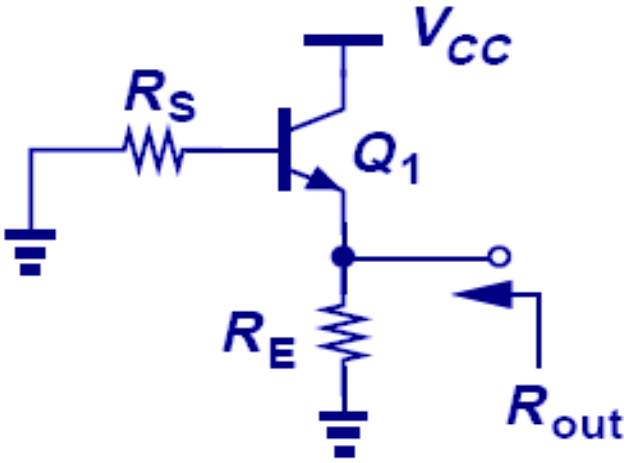
Thus, the voltage gain of the CE stage drops from 20 to $20\text{x}(R_C||R_{in1})/R_C = 10.28$, a substantial improvement over case (a).

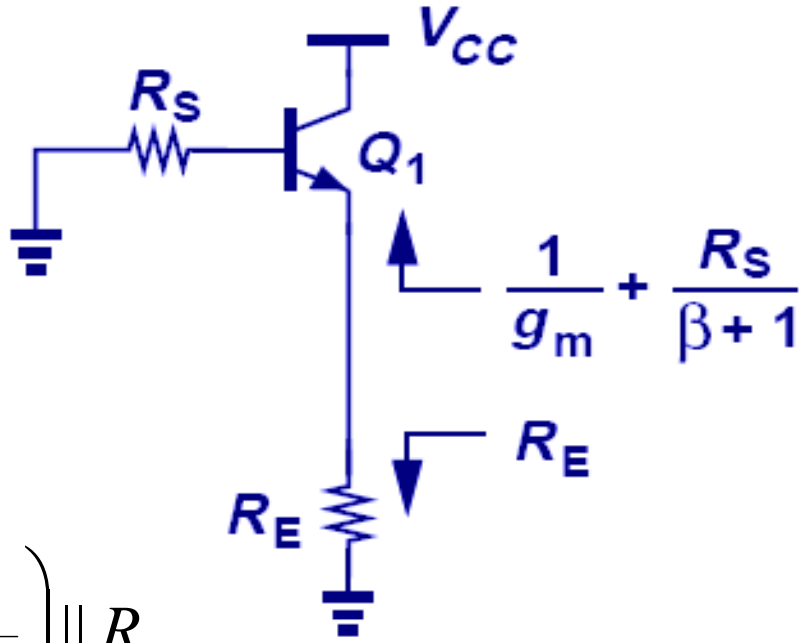




Output Impedance of Emitter Follower

- R_{out} can be viewed as the parallel combination of two components: one seen looking "up" into the emitter, $R_S/(\beta+1) + 1/g_m$, and another looking "down" into R_E.
- Emitter follower lowers the source impedance by a factor of β+1, improved driving capability.
- Good "***voltage buffer***" because it displays a high input impedance (like a voltmeter) and a low output impedance (like a voltage source).

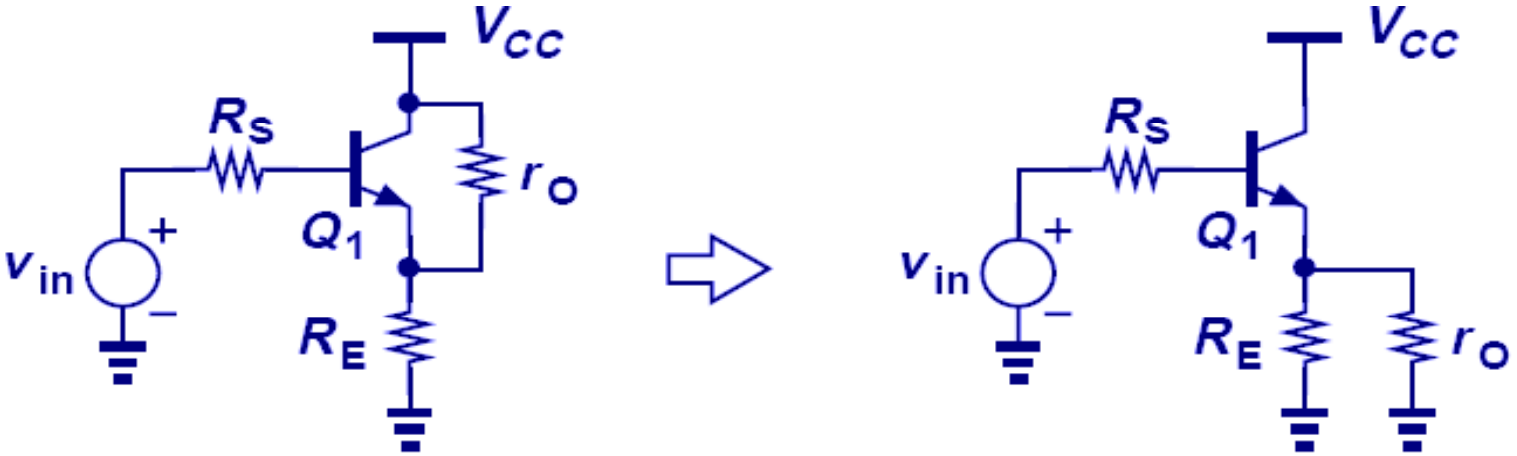




$$R_{out} = \left(\frac{R_s}{\beta+1} + \frac{1}{g_m} \right) \| R_E$$

Emitter Follower with Early Effect

- Since r_O is in parallel with R_E, its effect can be easily incorporated into voltage gain and input and output impedance equations.



$$A_v = \frac{R_E \parallel r_O}{R_E \parallel r_O + \dfrac{R_S}{\beta+1} + \dfrac{1}{g_m}}$$

$$R_{in} = r_\pi + (\beta+1)(R_E \parallel r_O)$$

$$R_{out} = \left(\frac{R_s}{\beta+1} + \frac{1}{g_m} \right) \parallel R_E \parallel r_O$$

Example 5.46

Determine the small-signal properties of an emitter follower using an ideal current source (as in Example 5.43) but with a finite source impedance R_S.

Solution

Since $R_E = \infty$, we have

$$A_v = \frac{r_O}{r_O + \dfrac{R_S}{\beta+1} + \dfrac{1}{g_m}}$$

$$R_{in} = r_\pi + (\beta+1)r_O) \qquad R_{out} = \left(\frac{R_S}{\beta+1} + \frac{1}{g_m}\right) \| \, r_O .$$

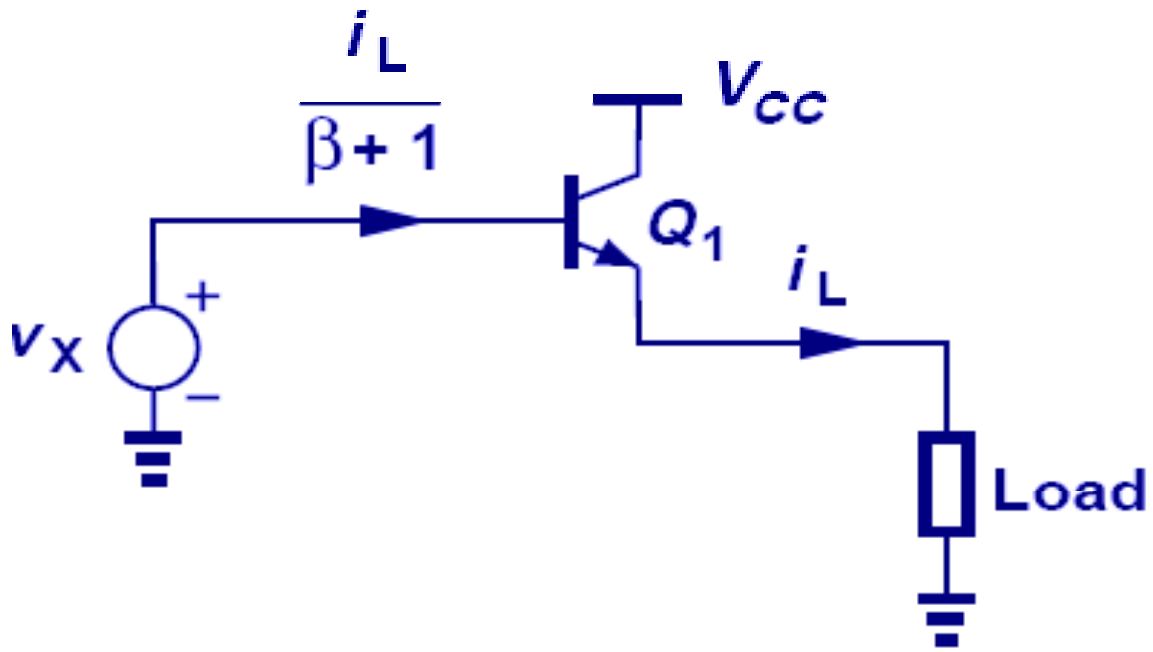
Also, $g_m r_O >> 1$, and hence

$$A_v \approx \frac{r_O}{r_O + \dfrac{R_S}{\beta+1}} \qquad R_{in} \approx (\beta+1)r_O .$$

We note that A_v approaches unity if $R_S << (\beta+1)r_O$, a condition typically valid.

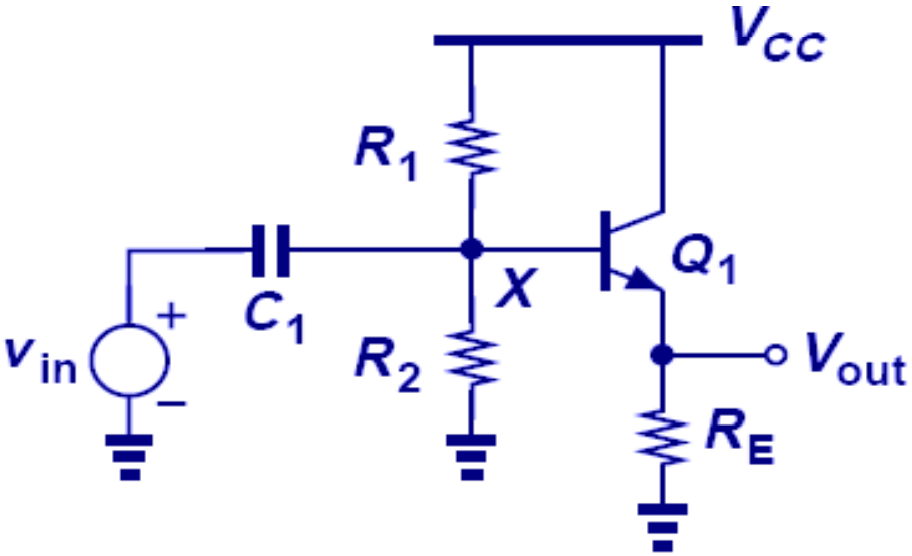
Current Gain

- There is a current gain of (β+1) from base to emitter.
- For a current i_L delivered to the load, the follower draws only $i_L/(\beta+1)$ from the source voltage.
- Effectively speaking, the load resistance is multiplied by (β+1) as seen from the base.

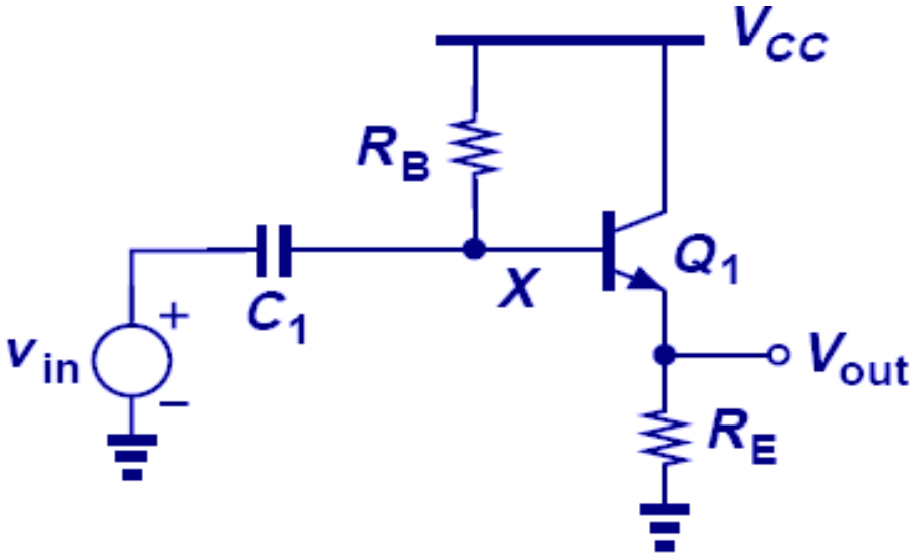


Emitter Follower with Biasing

- A biasing technique similar to that of CE stage can be used for the emitter follower.
- Also, V_b can be close to V_{CC} because the collector is also at V_{CC}.



the current flowing through R_1 and R_2 is chosen to be much greater than the base current.



$R_B I_B$ is chosen much less than the voltage drop across R_E, thus lowering the sensitivity to β

Example 5.47 Supply-Independent Biasing

The follower of Fig. 5.94(b) employs $R_B = 10\ \text{k}\Omega$ and $R_E = 1\ \text{k}\Omega$. Calculate the bias current and voltages if $I_S = 5\text{x}10^{-16}$ A, $\beta = 100$, and $V_{CC} = 2.5$ V. What happens if β drops to 50?

Solution

To determine the bias current, we follow the iterative procedure described in Section 5.2.3. Writing a KVL through R_B, the base-emitter junction, and R_E gives

$$\frac{R_B I_C}{\beta} + V_{BE} + R_E I_C = V_{CC},$$

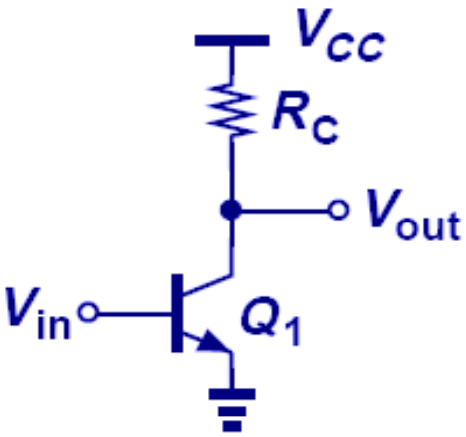
which, with $V_{BE} \approx 800$ mV, leads to $I_C = 1.545$ mA.
It follows that $V_{BE} = V_T \ln(I_C/I_S) \approx 748$mV. Using this value in Eq. (5.338), we have $I_C =$ 1.593 mA, close to1.545mA and hence relatively accurate. Under this condition, $I_B R_B =$ 159 mV whereas $I_C R_E = 1.593$V.

Since $I_B R_B << I_C R_E$, we expect that variation of β and hence $I_B R_B$ negligibly affects the voltage drop across R_E and hence the emitter and collector currents. As a rough estimate, for $\beta = 50$, $I_B R_B$ is doubled (≈ 318 mV), reducing the drop across R_E by 159 mV. That is, I_E = (1.593V - 0.159V)/1k Ω = 1.434 mA, implying that a twofold change in β leads to a change in the collector current. The reader is encouraged to repeat the above iterations with $\beta = 50$ and determine the exact current.

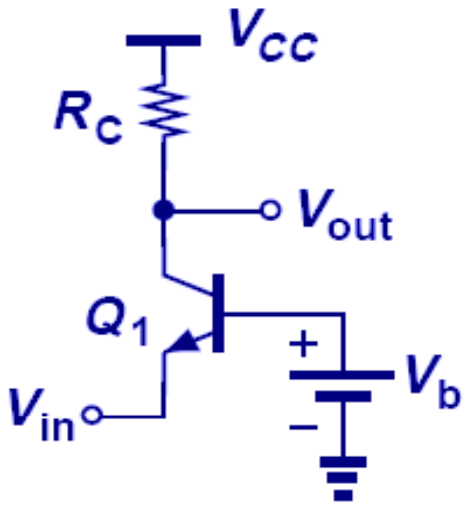
Summary of Amplifier Topologies

- The three amplifier topologies studied so far have different properties and are used on different occasions.
- CE and CB have voltage gain with magnitude greater than one, while follower's voltage gain is at most one.

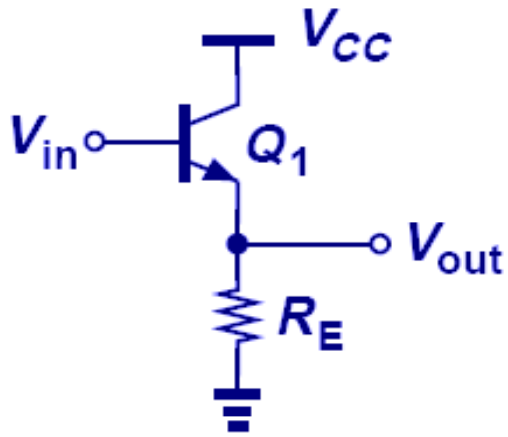
CE Stage



CB Stage

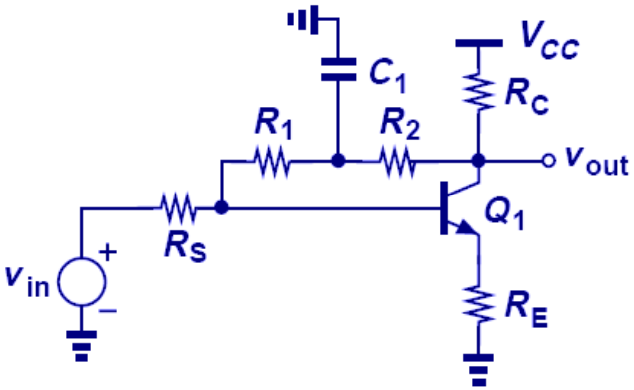


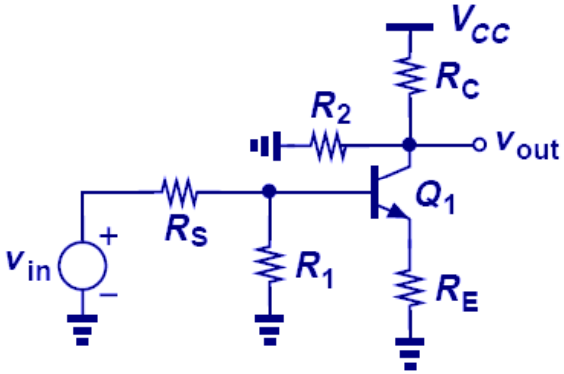
Follower

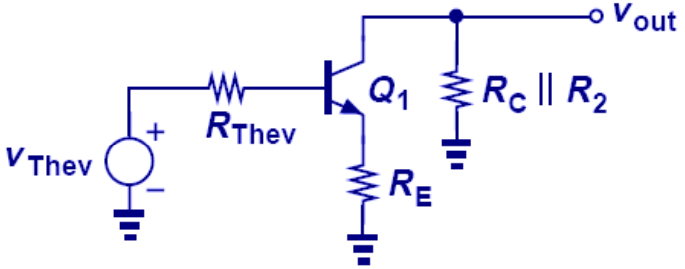


Amplifier Example I

- The keys in solving this problem are recognizing the AC ground between R_1 and R_2, and Thevenin transformation of the input network.







$$\frac{v_{out}}{v_{Thev}} = -\frac{R_2 \parallel R_C}{\frac{R_{Thev}}{\beta+1} + \frac{1}{g_m} + R_E}.$$

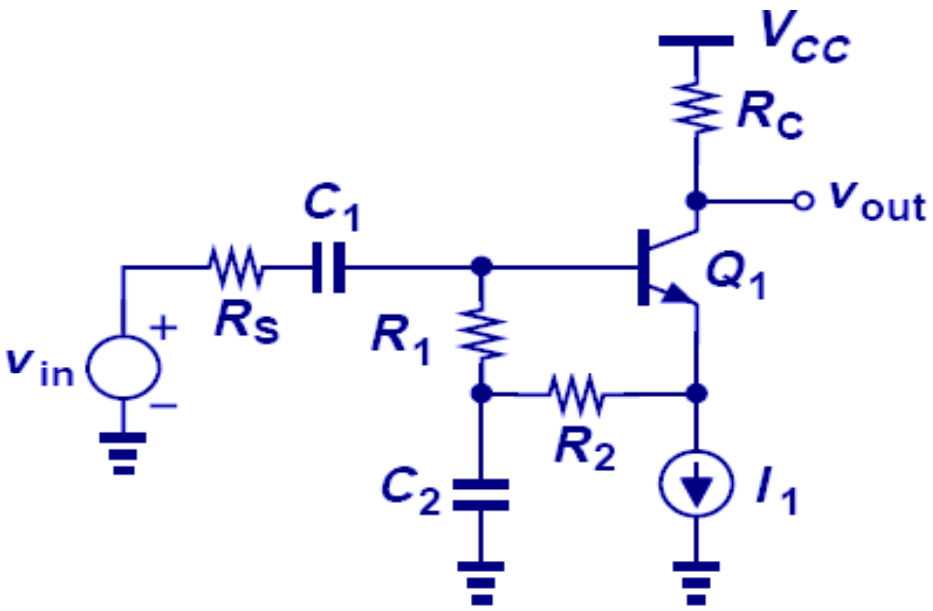
$$v_{Thev} = \frac{R_1}{R_1 + R_S} v_{in}$$

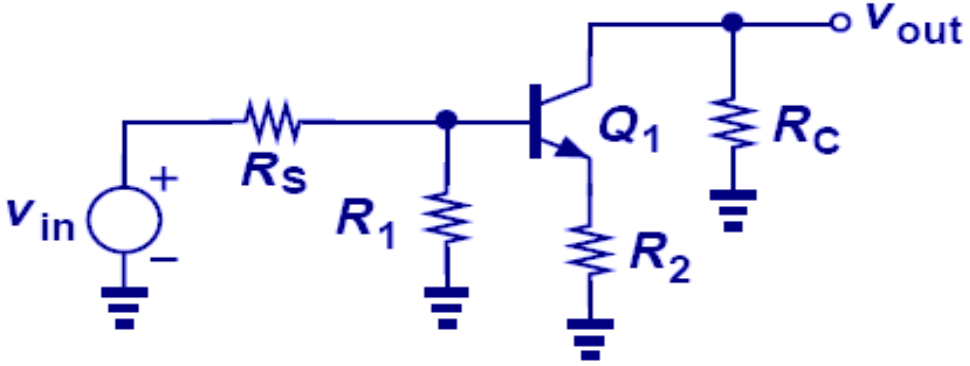
$$R_{Thev} = R_1 \parallel R_S.$$

$$\frac{v_{out}}{v_{in}} = -\frac{R_2 \parallel R_C}{\frac{R_1 \parallel R_S}{\beta+1} + \frac{1}{g_m} + R_E} \cdot \frac{R_1}{R_1 + R_S}$$

Amplifier Example II

- Again, AC ground/short and Thevenin transformation are needed to transform the complex circuit into a simple stage with emitter degeneration.



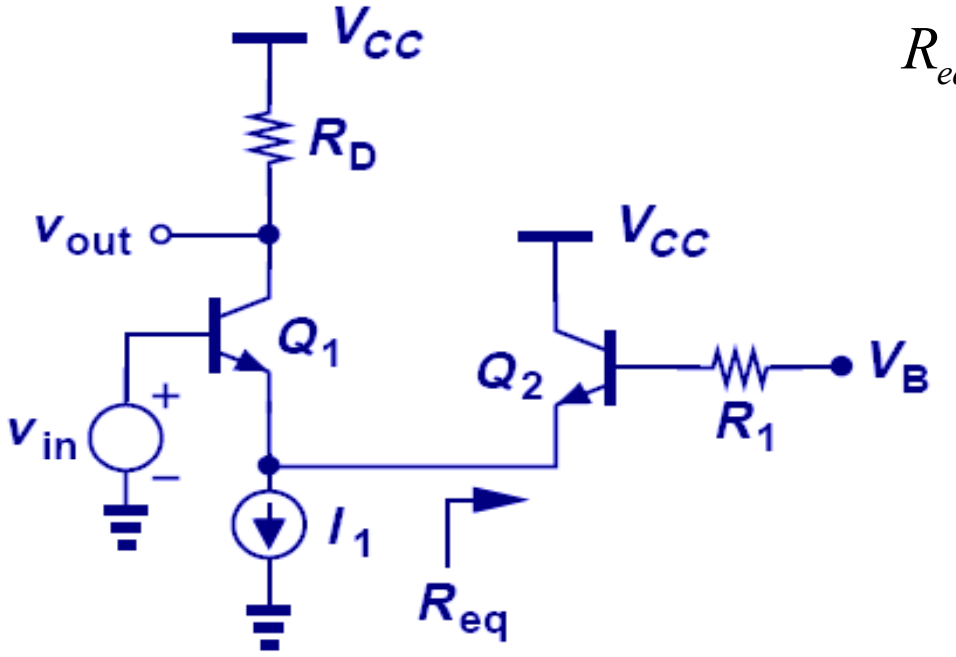


$$\frac{v_{out}}{v_{in}} = -\frac{R_C}{\frac{R_{Thev}}{\beta+1} + \frac{1}{g_m} + R_2}$$

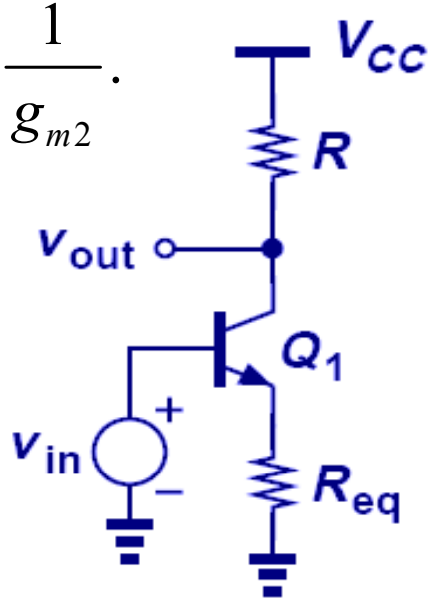
$$\frac{v_{out}}{v_{in}} = -\frac{R_C}{\frac{R_S \parallel R_1}{\beta+1} + \frac{1}{g_m} + R_2} \cdot \frac{R_1}{R_1 + R_S}$$

Amplifier Example III

- The key for solving this problem is first identifying R_{eq}, which is the impedance seen at the emitter of Q_2 in parallel with the infinite output impedance of an ideal current source. Second, use the equations for degenerated CE stage with R_E replaced by R_{eq}.



$$R_{eq} = \frac{R_1}{\beta+1} + \frac{1}{g_{m2}}.$$



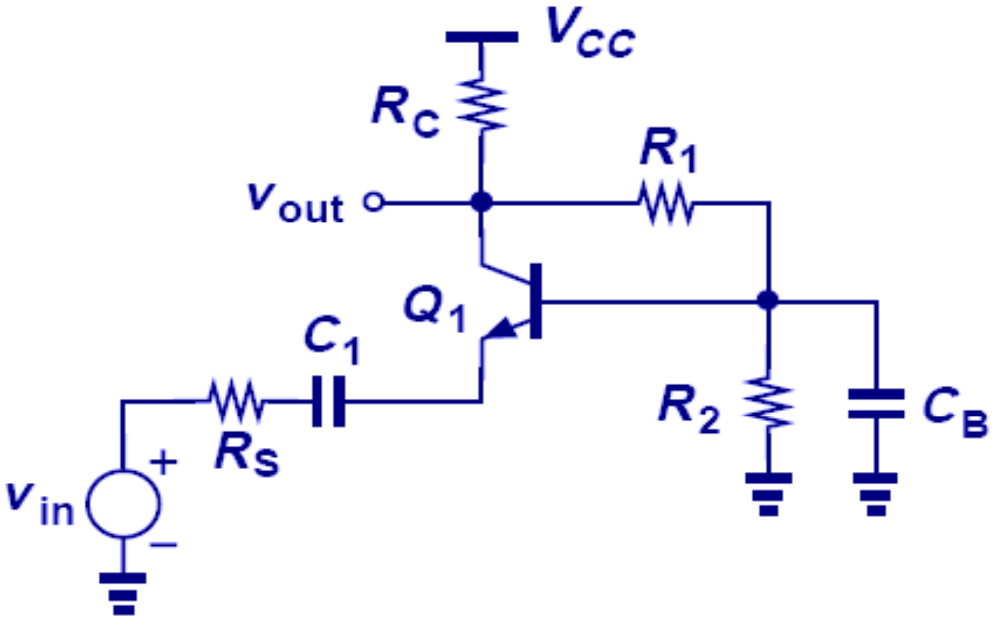
$$A_v = \frac{-R_C}{\frac{1}{g_{m1}} + R_{eq}} = \frac{-R_C}{\frac{1}{g_{m1}} + \frac{R_1}{\beta+1} + \frac{1}{g_{m2}}}.$$

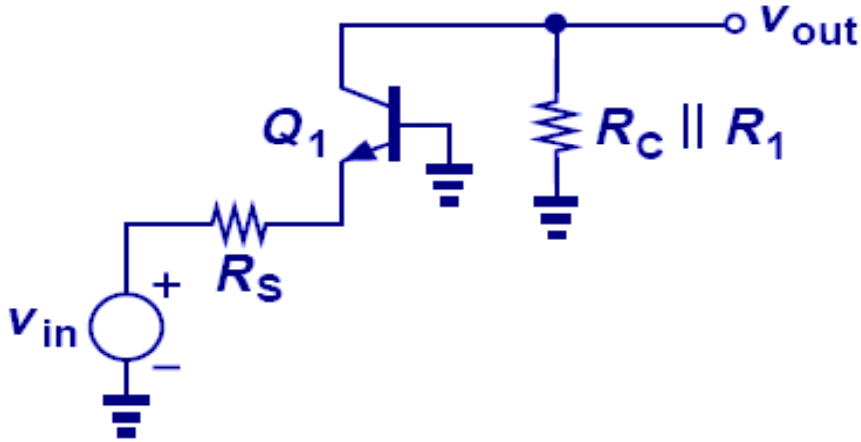
$$R_{in} = r_{\pi 1} + (\beta+1)R_{eq}$$

$$= r_{\pi 1} + R_1 + r_{\pi 2}.$$

Amplifier Example IV

- The key for solving this problem is recognizing that C_B at frequency of interest shorts out R_2 and provide a ground for R_1.
- R_1 appears in parallel with R_C and the circuit simplifies to a simple CB stage.

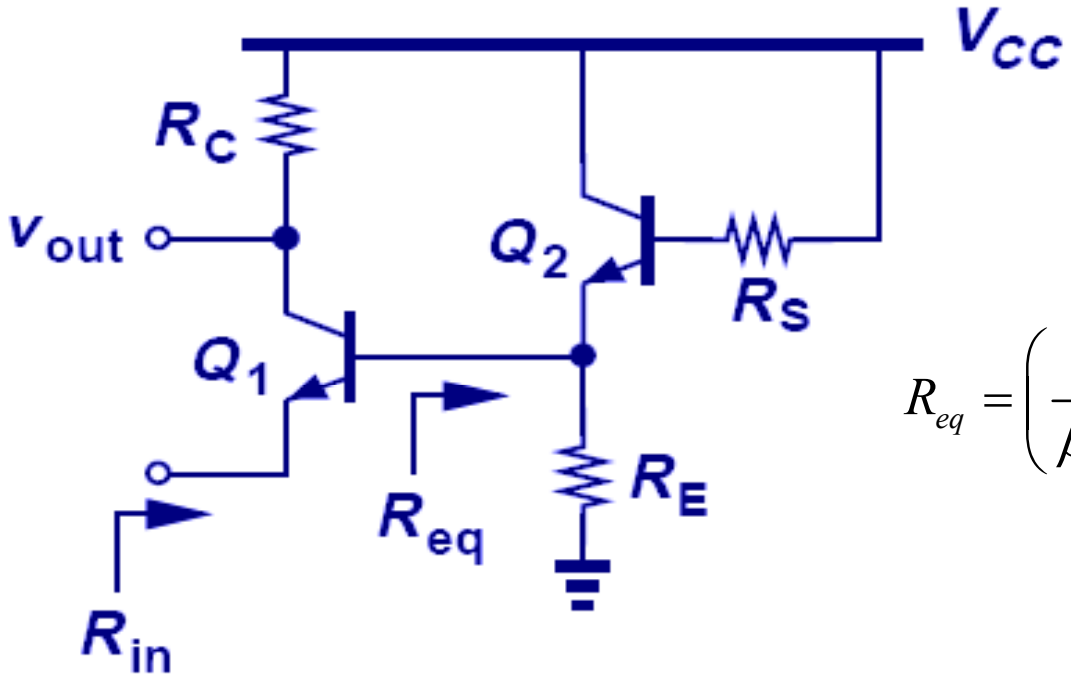




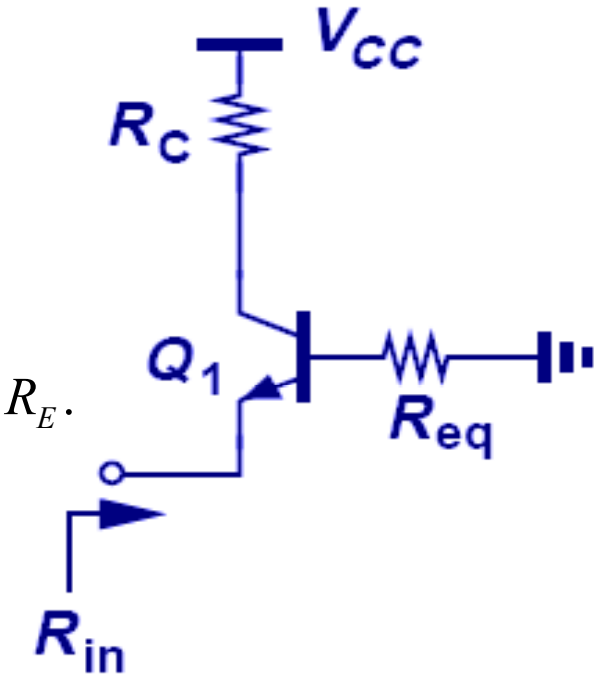
$$A_v = \frac{R_C \parallel R_1}{R_S + \dfrac{1}{g_m}}$$

Amplifier Example V

- The key for solving this problem is recognizing the equivalent base resistance of Q_1 is the parallel connection of R_E and the impedance seen at the emitter of Q_2.



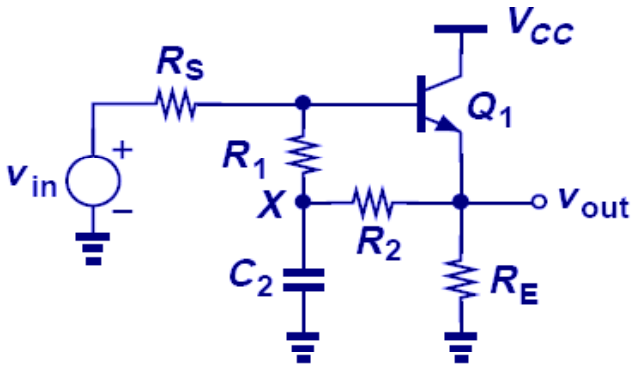
$$R_{eq} = \left(\frac{R_B}{\beta + 1} + \frac{1}{g_{m2}} \right) \| R_E .$$



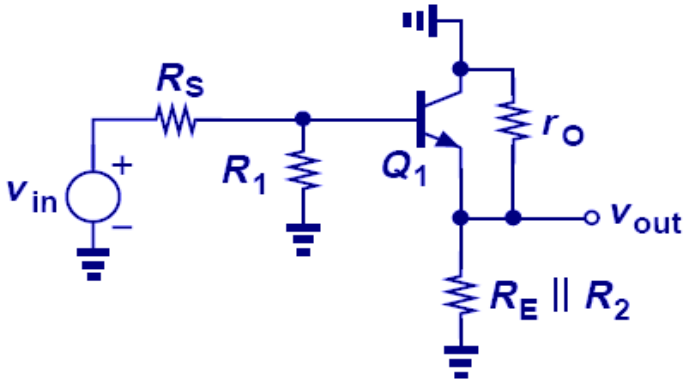
$$R_{in} = \frac{R_{eq}}{\beta + 1} + \frac{1}{g_{m1}} = \frac{1}{\beta + 1} \left[\left(\frac{R_B}{\beta + 1} + \frac{1}{g_{m2}} \right) \| R_E \right] + \frac{1}{g_{m1}} .$$

Amplifier Example VI

- The key in solving this problem is recognizing a DC supply is actually an AC ground and using Thevenin transformation to simplify the circuit into an emitter follower.

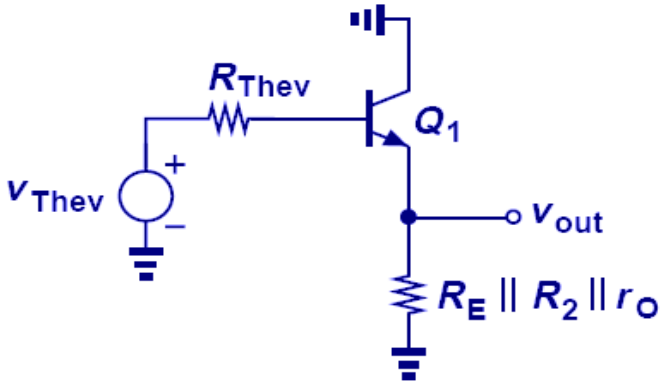


(a)



(b)

$$\frac{v_{out}}{v_{Thev}} = \frac{R_E \parallel R_2 \parallel r_O}{R_E \parallel R_2 \parallel r_O + \frac{1}{g_m} + \frac{R_{Thev}}{\beta+1}}$$



(c)

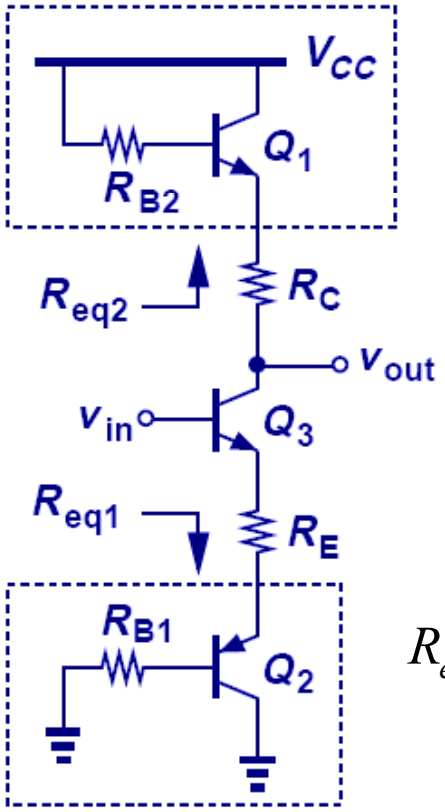
$$\frac{v_{out}}{v_{in}} = \frac{R_E \parallel R_2 \parallel r_O}{R_E \parallel R_2 \parallel r_O + \frac{1}{g_m} + \frac{R_S \parallel R_1}{\beta+1}} \cdot \frac{R_1}{R_1 + R_S}$$

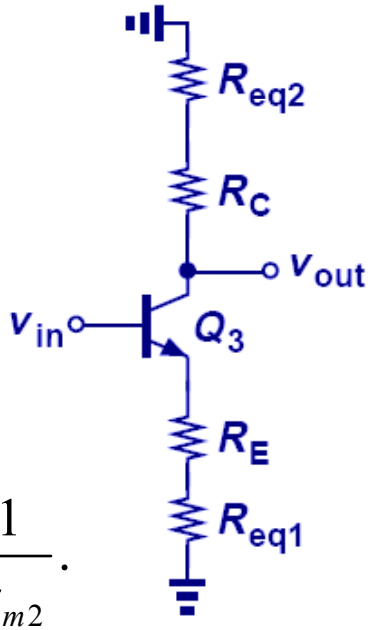
$$R_{out} = \left(\frac{R_{Thev}}{\beta+1} + \frac{1}{g_m} \right) \parallel (R_E \parallel R_2 \parallel r_O)$$

$$R_{out} = \left(\frac{R_S \parallel R_1}{\beta+1} + \frac{1}{g_m} \right) \parallel R_E \parallel R_2 \parallel r_O$$

Amplifier Example VII

- Impedances seen at the emitter of Q_1 and Q_2 can be lumped with R_C and R_E, respectively, to form the equivalent emitter and collector impedances.





$$R_{eq1} = \frac{R_{B1}}{\beta+1} + \frac{1}{g_{m2}}.$$

$$R_{eq2} = \frac{R_{B2}}{\beta+1} + \frac{1}{g_{m1}},$$

$$R_{in} = r_{\pi 3} + (\beta+1)(R_E + R_{eq1})$$

$$R_{out} = R_C + R_{eq2}$$

$$A_v = -\frac{R_C + R_{eq2}}{R_{eq1} + \frac{1}{g_{m3}} + R_E}$$

$$R_{in} = r_{\pi 1} + (\beta+1)\left(R_E + \frac{R_{B1}}{\beta+1} + \frac{1}{g_{m2}}\right)$$

$$R_{out} = R_C + \frac{R_{B2}}{\beta+1} + \frac{1}{g_{m3}}$$

$$A_v = -\frac{R_C + \frac{R_{B2}}{\beta+1} + \frac{1}{g_{m3}}}{\frac{R_{B1}}{\beta+1} + \frac{1}{g_{m2}} + \frac{1}{g_{m1}}}$$

Example

Objective：Analyze a pnp amplifier circuit. Assume transistor parameters of β=80, $V_{EB}(on)$=0.7V, and V_A=∞.

Solution (DC Analysis): A dc KVL equation around the E-B loop yields

$$V^+ = V_{EB}(on) + I_{BQ}R_B + V_{BB} \quad \text{or} \quad 5 = 0.7 + I_{BQ}(50) + 3.65$$

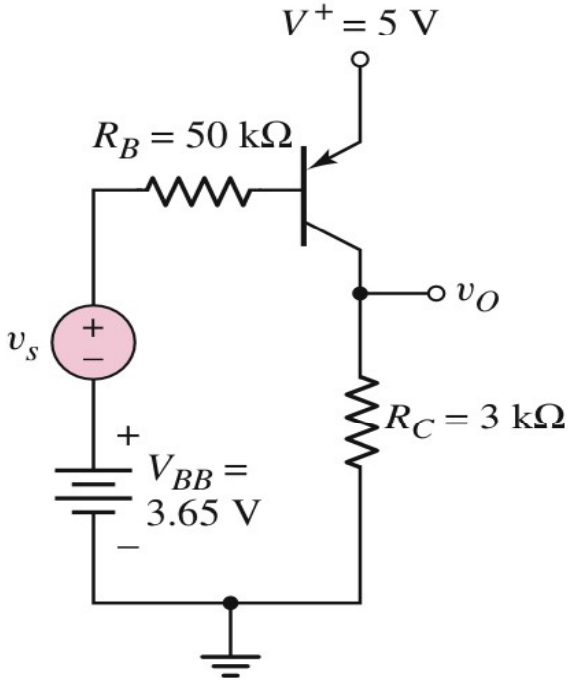
which yields $I_{BQ} = 13\mu A$

Then $I_{CQ} = 1.04mA, \quad I_{EQ} = 1.05mA$

A dc KVL equation around the E-C loop yields

$$V^+ = V_{ECQ} + I_{BQ}R_C \quad \text{or} \quad 5 = V_{ECQ} + (1.04)(3)$$

We find $V_{ECQ} = 1.88V$



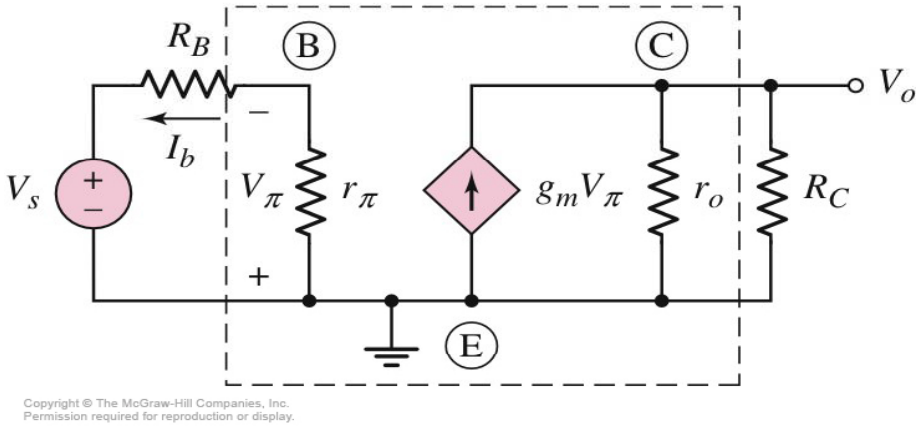
The transistor is therefore biased in the forward-active mode.

Solution (AC Analysis): The small-signal hybrid-π parameters are found to be

$$g_m = \frac{I_{CQ}}{V_T} = \frac{1.04}{0.026} = 40mA/V \qquad r_\pi = \frac{\beta V_T}{I_{CQ}} = \frac{(80)(0.026)}{1.04} = 2k\Omega$$

and $$r_0 = \frac{V_A}{I_{CQ}} = \frac{\infty}{1.04} = \infty$$

The small-signal equivalent circuit is shown in Figure
With $r_o=\infty$, the small-signal output voltage is



$$V_0 = (g_m V_\pi) R_C \quad \text{and} \quad V_\pi = -\left(\frac{r_\pi}{r_\pi + R_B}\right) V_S$$

Noting that β= $g_m r_\pi$, we find the small-signal voltage gain to be

$$A_v = \frac{V_0}{V_s} = \frac{-\beta R_C}{r_\pi + R_B} = \frac{-(80)(3)}{2+50} \quad \text{or} \quad A_v = -4.62$$

- The samll-signal input resistance seen by the signal source (see the Figure) is

$$R_i = R_B + r_\pi = 50 + 2 = 52k\Omega$$

- The samll-signal output resistance looking back into the output terminal is

$$R_o = R_C \| r_o = 3 \| \infty = 3k\Omega$$

- Comment : We again note the -180^o phase shift between the output and input signals. We may also note that the base resistance R_B in the denominator substantially reduces the magnitude of the small-signal voltage gain. We can also note that placing the pnp transistor in this configuration allows us to use positive power supplies.

Three Basic Amplifiers: summary and comparison

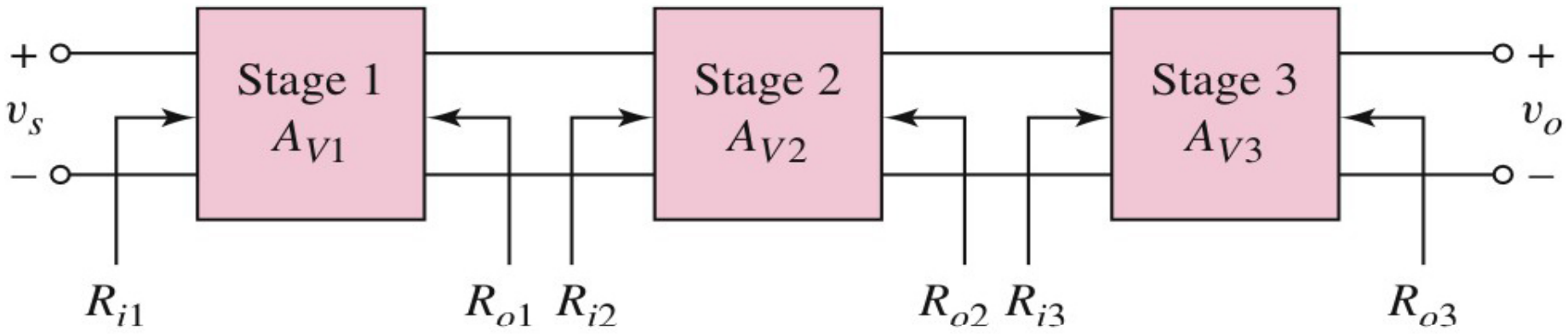
Characteristics of the three BJT amplifier configurations

Configuration	Voltage gain	Current gain	Input resistance	Output resistance
Common emitter	$A_v > 1$	$A_i > 1$	Moderate	Moderate to high
Emitter follower	$A_v \cong 1$	$A_i > 1$	High	Low
Common base	$A_v > 1$	$A_i \cong 1$	Low	Moderate to high

- This table will be used in the design of multistage amplifiers

Multistage Amplifiers

- Transistor amplifiers circuits in series or cascade



- Increase voltage gain
- Very low output resistance

Cascade Configuration

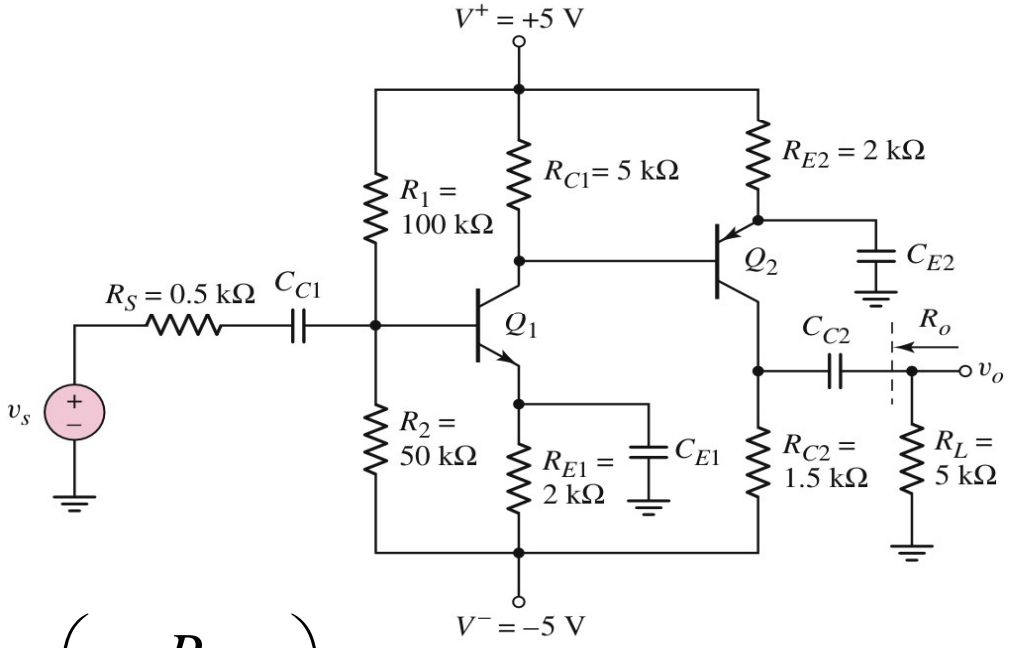
each transistor $r_o = 0$

- Input resistance

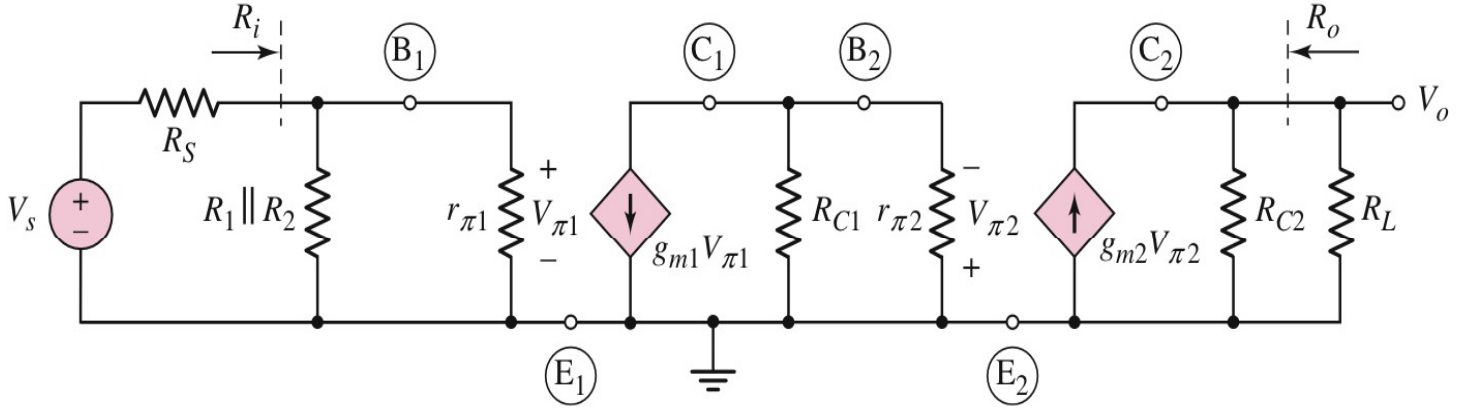
$$R_i = R_1 \| R_2 \| r_{\pi 1}$$

- Output resistance

$$v_s \Rightarrow 0,\ R_O = R_{c2}$$



$$A_v = \frac{v_o}{v_s} = g_{m1} g_{m2} \left(R_{c1} \| r_{\pi 2} \right) \left(R_{c2} \| R_L \right) \left(\frac{R_i}{R_i + R_s} \right)$$



Darlington Pair Configuration

$$v_{\pi 1} = I_i r_{\pi 1}$$

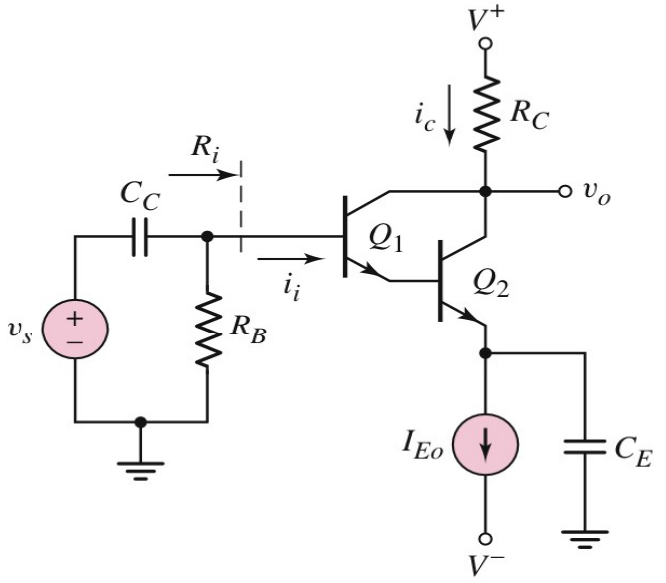
$$g_m v_{\pi 1} = g_{m1} r_{\pi 1} I_i = \beta_1 I_i$$

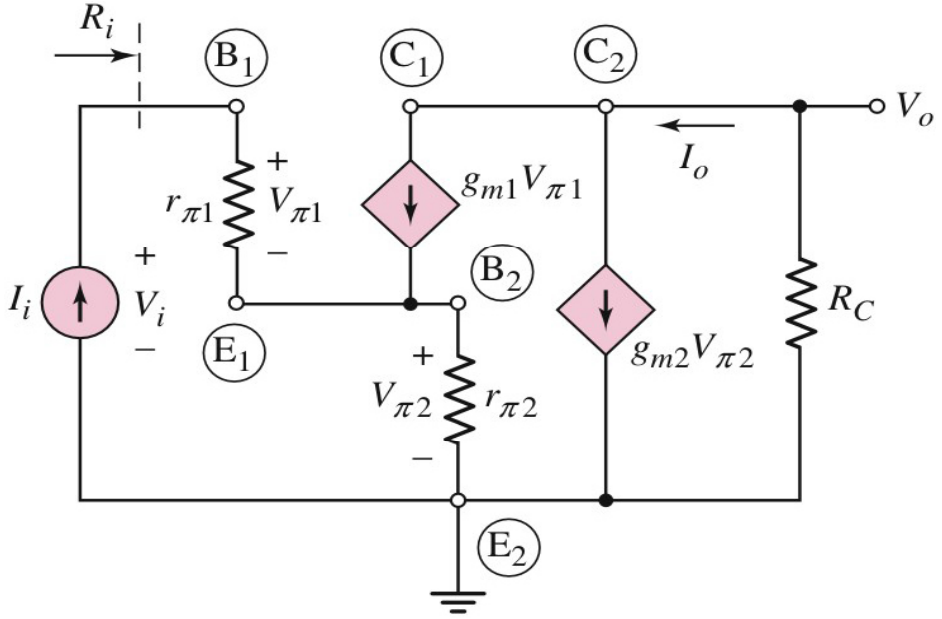
$$v_{\pi 2} = \left(I_i + \beta_1 I_i\right) r_{\pi 2}$$

$$I_o = g_{m1} v_{\pi 1} + g_{m2} v_{\pi 2}$$

$$= \beta_1 I_i + \beta_2 \left(I_i + \beta_1 I_i\right)$$

$$A_i = \frac{I_o}{I_i} = \beta_1 + \beta_2 \left(1 + \beta_1\right) \cong \beta_1 \beta_2$$





$$v_i = I_i r_{\pi 1} + I_i \left(1 + \beta_1\right) r_{\pi 2}$$

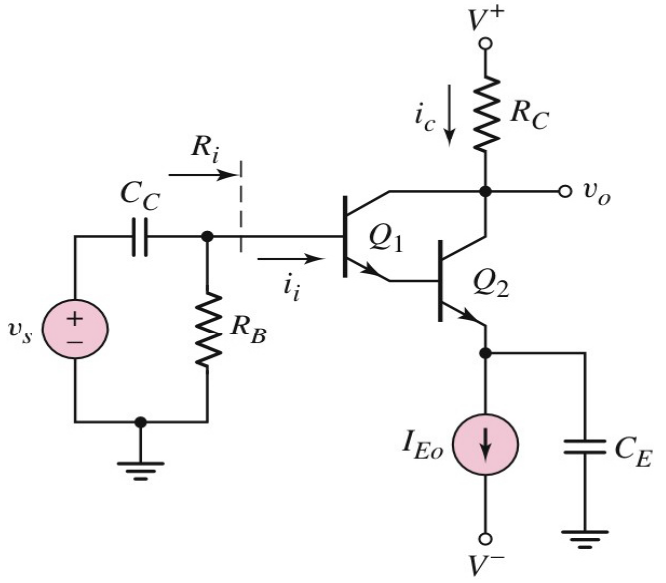
$$R_i = \frac{v_i}{I_i} = r_{\pi 1} + \left(1 + \beta_1\right) r_{\pi 2}$$

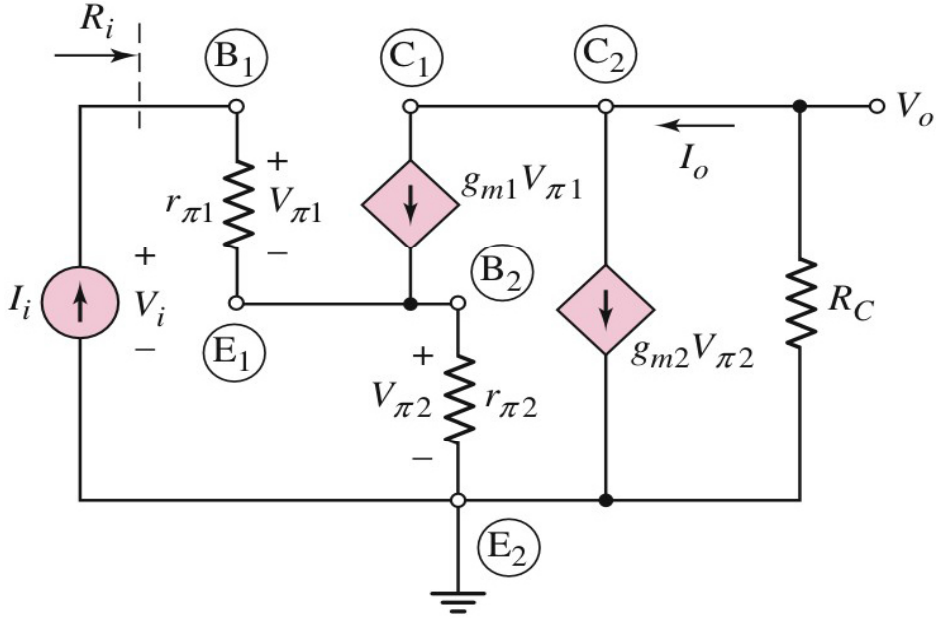
In another way,

$$r_{\pi 1} = \frac{\beta_1 v_T}{I_{CQ1}} \qquad I_{CQ1} \cong \frac{I_{CQ2}}{\beta_2}$$

$$r_{\pi 1} = \beta_1 \left(\frac{\beta_2 v_T}{I_{CQ2}} \right) = \beta_1 r_{\pi 2}$$

$$R_i \cong 2\beta_1 r_{\pi 2}$$





Cascode Configuration

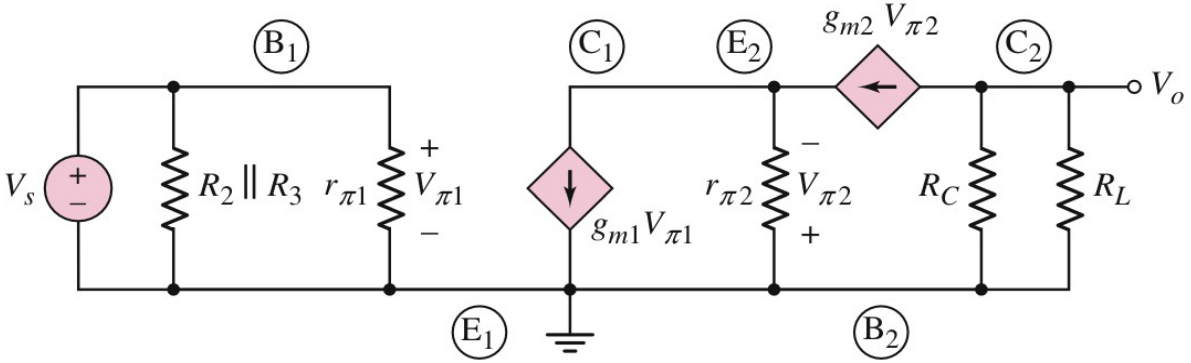
- Q_1 drives Q_2
- Output resistance is much larger
- The small signal gain

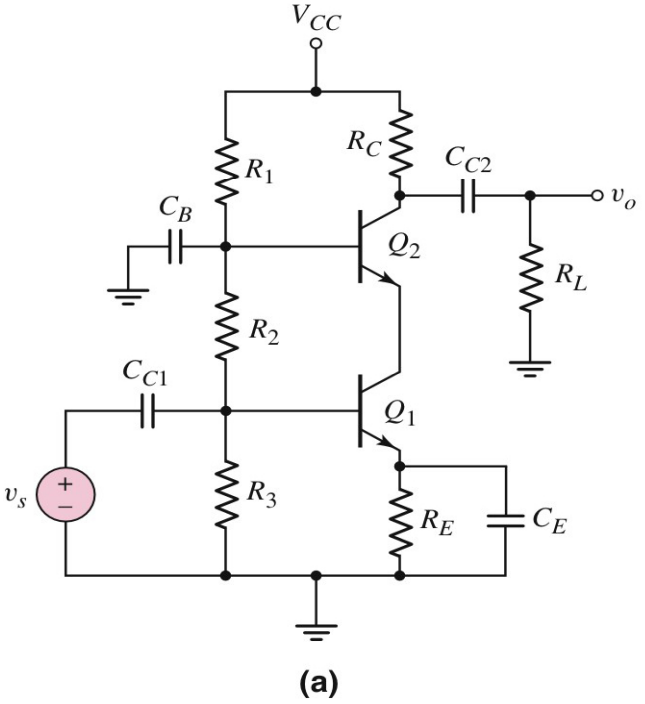
$$V_o = -(g_{m2}V_{\pi 2})(R_C \| R_L)$$

or

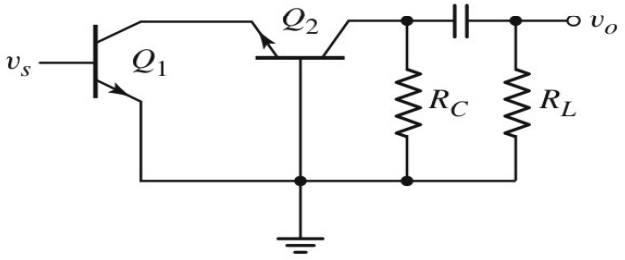
$$V_o = -g_{m1}g_{m2}\left(\frac{r_{\pi 2}}{1+\beta_2}\right)(R_C \| R_L)V_S$$

$$A_\upsilon = \frac{V_o}{V_S} = -g_{m1}g_{m2}\left(\frac{r_{\pi 2}}{1+\beta_2}\right)(R_C \| R_L)$$





(a)



(b)

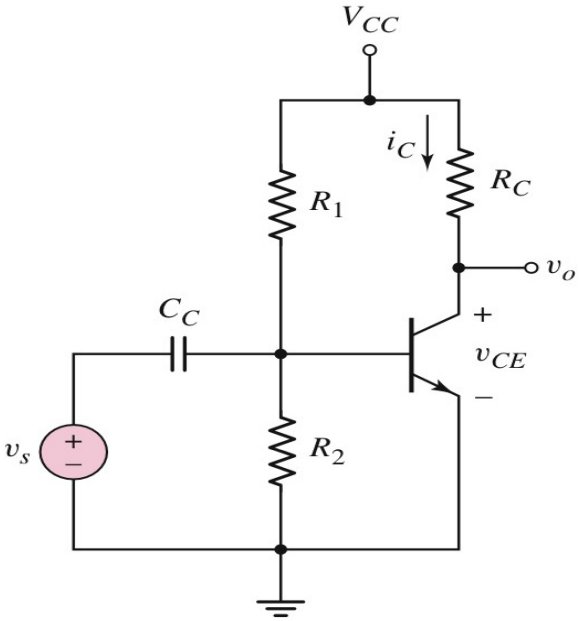
Power Considerations

- Energy must be conserved
- DC power

$$P_{CC} = I_{CQ}V_{CC} + P_{\text{Bias}}$$

$$P_{RC} = I_{CQ}^2 R_C$$

$$P_Q = I_{CQ}V_{CEQ} + I_{BQ}V_{BEQ} \approx I_{CQ}V_{CEQ}$$



- Power supplied by the voltage source

$$\overline{p}_{cc} = \frac{1}{T}\int_0^T V_{CC}\, i_C\, dt + P_{\text{Bias}} = \frac{1}{T}\int_0^T V_{CC}\,[I_{CQ} + I_c \cos \omega t]dt + P_{\text{Bias}}$$

$$= V_{CC}\, I_{CQ} + \frac{V_{CC}\, I_c}{T}\int_0^T \cos \omega t dt + P_{\text{Bias}}$$

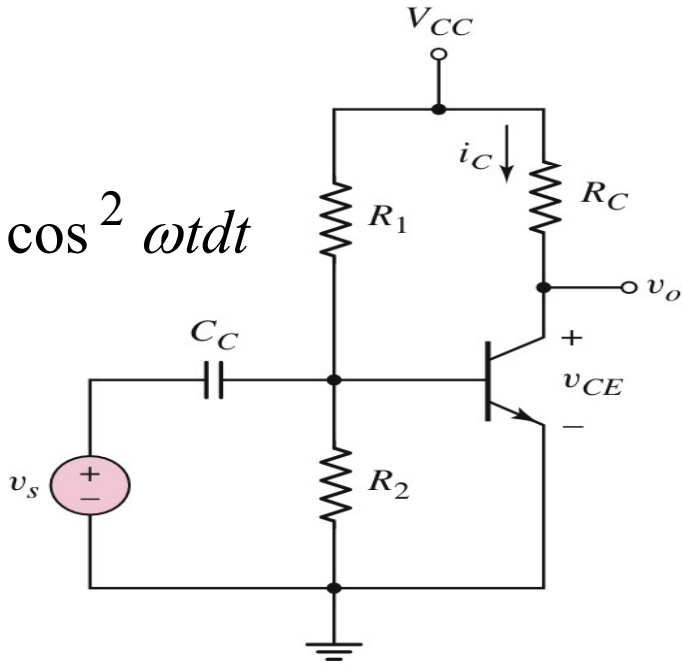
$$= I_{CQ}V_{CC} + P_{\text{Bias}} = P_{CC}$$

- Power delivered to the load R_c

$$\overline{p}_{RC} = \frac{1}{T}\int_0^T i_C^2 R_C\, dt = \frac{R_C}{T}\int_0^T [I_{CQ} + I_c \cos \omega t]^2\, dt$$

$$= \frac{I_{CQ}^2 R_C}{T}\int_0^T dt + \frac{2I_{CQ} I_c R_C}{T}\int_0^T \cos \omega t dt + \frac{I_c^2 R_C}{T}\int_0^T \cos^2 \omega t dt$$

$$= I_{CQ}^2 R_C + \frac{I_c^2 R_C}{2} = P_{RC} + \frac{I_c^2 R_C}{2}$$



- Power dissipated in the transistor

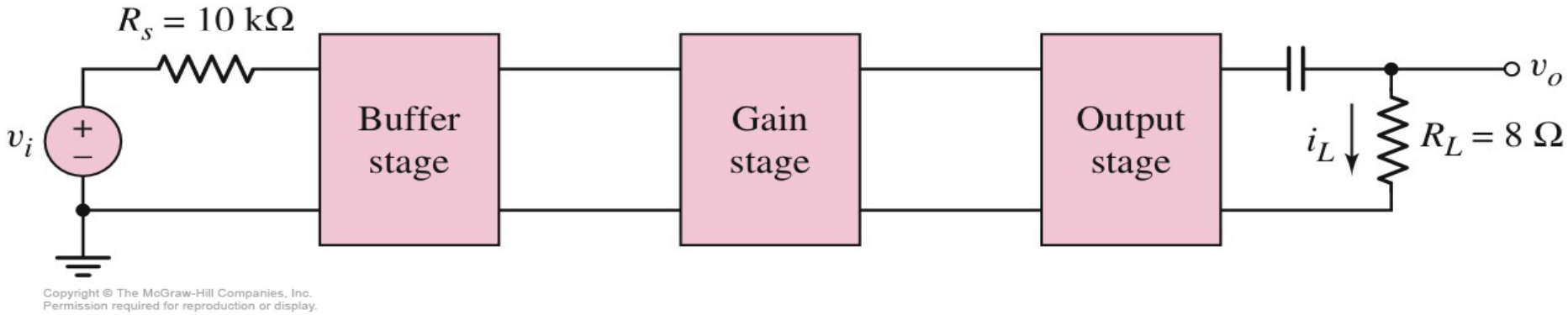
$$\overline{p}_Q = \frac{1}{T}\int_0^T i_C v_{CE}\, dt = \frac{1}{T}\int_0^T [I_{CQ} + I_c \cos \omega t][V_{CEQ} - I_c R_C \cos \omega t] dt$$

$$= I_{CQ} V_{CEQ} - \frac{I_c^2 R_C}{T}\int_0^T \cos^2 \omega t dt$$

$$= I_{CQ} V_{CEQ} - \frac{I_c^2 R_C}{2} = P_Q - \frac{I_c^2 R_C}{2}$$

Design Application : Audio Amp

- Design Approach



- Input : C-C circuit
  - Reduce loading effect
- Output : C-C circuit
  - Provide output current and output signal power
- Gain stage : 2-stage C-E
  - Provide voltage gain

Input buffer stage

$$\beta_1 = 100, I_{CQ1} = 1mA, V_{CEQ} = 6V, R_1 \,||\, R_2 = 100k\Omega$$

$$R_{E1} \cong \frac{V_{CC} - V_{CEQ1}}{I_{CQ1}} = 6k\Omega$$

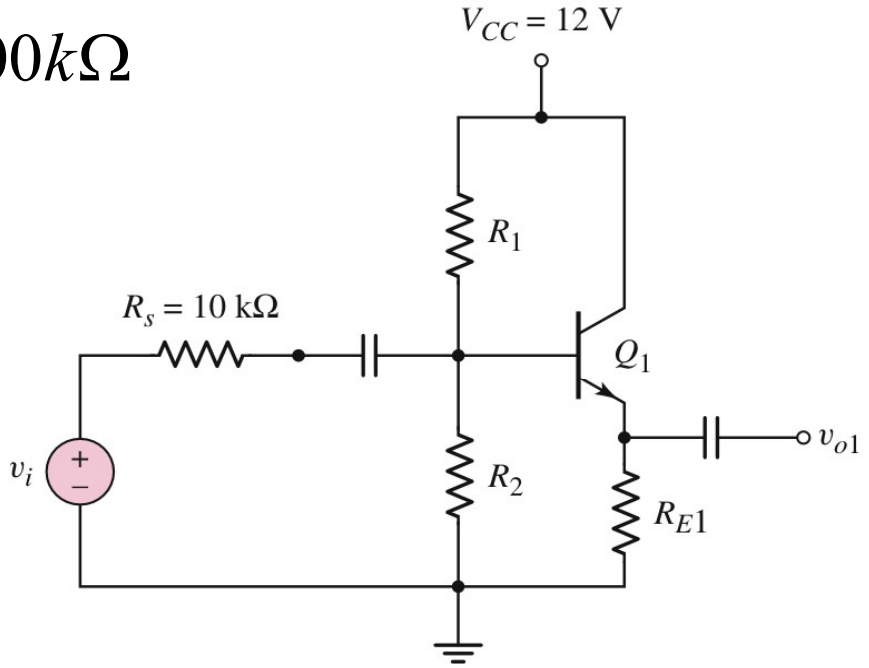
$$r_{\pi 1} = \frac{\beta_1 V_T}{I_{CQ1}} = 2.6k\Omega$$

$$R_{i1} = R_1 \,||\, R_2 \,||\left[r_{\pi 1} + \left(1+\beta_1\right) R_{E1} \right]$$

$$A_{v1} = \frac{v_{o1}}{v_i} = \frac{\left(1+\beta_1\right) R_{E1}}{r_{\pi 1} + \left(1+\beta_1\right) R_{E1}} \cdot \left(\frac{R_{i1}}{R_{i1} + R_s} \right) = 0.892$$

for input signal $10mV \rightarrow V_{o1} = 8.92mV$

$$\Rightarrow R_1 = 155k\Omega, R_2 = 282k\Omega$$



Output stage

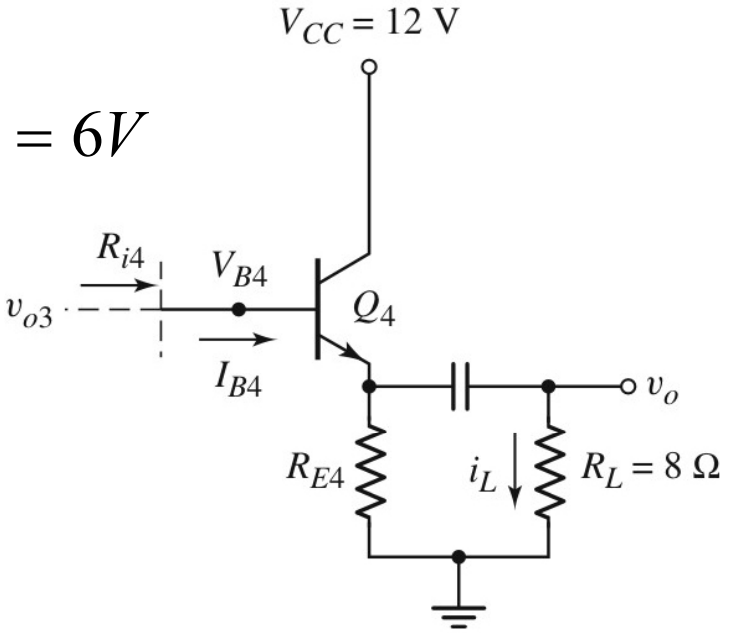
$$R_L = 8\Omega, P_L = 0.1W, \beta_4 = 50, I_{EQ4} = 0.3A, V_{CEQ4} = 6V$$

$$P_L = i_L{}^2(rms) \cdot R_L \rightarrow i_L(rms) = 0.112A$$

$$i_L(peak) = 0.158A$$

$$V_o(peak) = (0.158)(8) = 1.26V$$

$$R_{E4} = \frac{V_{CC} - V_{CEQ4}}{I_{EQ4}} = 20\Omega$$



$$I_{CQ4} = \left(\frac{\beta_4}{1+\beta_4}\right) \cdot I_{EQ4} = 0.294A$$

$$A_{V4} = \frac{v_o}{v_{o3}} = \frac{(1+\beta_4)(R_{E4} \parallel R_L)}{r_{\pi 4} + (1+\beta_4)(R_{E4} \parallel R_L)}$$

$$r_{\pi 4} = \frac{\beta_4 V_T}{I_{CQ4}} = 4.42\Omega$$

$$\because v_o = 1.26V \rightarrow v_{o3} = 1.28V$$

Gain stage

$$\beta = 100, \left|\frac{v_{o3}}{v_{o1}}\right| = \frac{1.28}{0.00892} = 144, \left|A_{v3}\right| = \left|\frac{v_{o3}}{v_{o2}}\right| = 5, \left|A_{v2}\right| = \left|\frac{v_{o2}}{v_{o1}}\right| = 28.8,$$

$$R_5 \parallel R_6 = 50k, R_3 \parallel R_4 = 50k, V_{C2} = 6V, I_{CQ2} = 5mA$$

$$\left|A_{v3}\right| = \frac{\beta_3 \left(R_{C3} \parallel R_{i4}\right)}{r_{\pi 3} + \left(1+\beta_3\right) R_{E3}}$$

$$\rightarrow R_{E3} = 25.4\Omega$$

$$\left|A_{v2}\right| = \frac{\beta 2 \left(R_{C2} \parallel R_{i3}\right)}{r_{\pi 2} + \left(1+\beta_2\right) R_{E2}}$$

$$\rightarrow R_{E2} = 23.1\Omega$$